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Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, January 1 to December 31, 1977

F. F. Oettinger, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, D.C. 20234

April 1978

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Division of Electric Energy Systems
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TABLE OF CONTENTS

	Page
EXECUTIVE SUMMARY	1
1. Introduction	6
2. Photovoltaic Technique	7
2.1 Objectives	7
2.2 Background	8
2.2.1 Importance of Resistivity and Resistivity Variation for Power Devices	8
2.2.2 Limitations of Present Method	8
2.2.3 Photovoltaic Technique	8
2.3 Review of Past Accomplishments	9
2.4 Accomplishments This Year	9
2.4.1 System Characterization	16
2.4.1.1 Illumination Wavelength	16
2.4.1.2 Surface Finish	17
2.4.1.3 Measurement Time	17
2.4.1.4 Theoretical Analysis	18
2.4.1.5 Experimental Results	23
2.4.1.6 Extension to NTD Silicon	23
2.4.2 Dissemination of Results	27
3. Deep Level Measurements	30
3.1 Objectives	30
3.2 Background	31
3.3 Accomplishments This Year	31
3.3.1 Test Structure Development	31
3.3.2 Utilization of Thermally Stimulated Measurements for the Detection of Defects	38
3.3.2.1 Analysis of Defect Levels	40
3.3.2.2 Separation of Electron and Hole Emission Rates	46
3.3.2.3 Ion Implantation as a Means for Introducing Defect Centers in Silicon	50
3.3.3 Extension of Thermally Stimulated Measurement Techniques to Deep Level Transient and Defect Profiling Measurements	51
3.3.3.1 Transient Capacitance Technique	51
3.3.3.2 Defect Profiling Technique	59

Page

3.3.4 Correlation of Defect Density with Electrical Parameters 62

4. Spreading Resistance Measurements 69

4.1 Objectives 69

4.2 Background 69

4.3 Status 74

4.3.1 Surface Preparation Procedures for Radial Profiling 74

4.3.2 Surface Preparation Procedures for Depth Profiling 74

4.3.3 Dopant Species Dependence of Calibration for *p*-Type Silicon 74

5. References 75

LIST OF FIGURES

2-1. Photograph of automated photovoltaic resistivity gradient measurement system 10

2-2. Schematic of automated photovoltaic system 11

2-3. Schematic of computer-controlled measurement circuitry . . . 12

2-4. Photograph of specimen holder used with the photovoltaic system 14

2-5. Schematic of one of the pneumatic probe-lowering systems . . 15

2-6. Slice geometry used for van der Pauw average resistivity measurement 16

2-7. Geometry for theoretical calculations 20

2-8. Comparison of four-probe and photovoltaic resistivity profiles for an *n*-type silicon slice of nominal resistivity of 150 Ω·cm 24

2-9. Comparison of four-probe and photovoltaic resistivity profiles for an *n*-type silicon slice of nominal resistivity of 10 Ω·cm 25

2-10. Comparison of four-probe and photovoltaic resistivity profiles for an NTD specimen with normal resistivity gradient 26

2-11. Comparison of four-probe and photovoltaic resistivity profiles for an NTD specimen with an abnormally large resistivity gradient 28

Page

3-1a. Photographs of levels 1 through 4 of the NBS-13 mesa diode mask set 35

3-1b. Photographs of levels 5 through 8 of the NBS-13 mesa diode mask set 36

3-2. A mesa diode fabrication procedure using five mask levels to separate the n- and p^+-metallization steps . . . 37

3-3. Photomicrograph of one cell of a plasma-etched wafer using the NBS-13 mask set 39

3-4. Thermally stimulated capacitance and current responses of sulfur defect centers in n-type silicon at nominal heating rates of 10, 5, and 2 K/s and zero 41

3-5. Representative isothermal transient capacitance response of a reverse-biased p^+n junction 44

3-6. Representative semilog plot of capacitance ratio, C_r, against time 45

3-7. Semilog plots of reduced emission rates against inverse temperature for two energy levels of sulfur in n-type silicon 47

3-8. Schematic representation of the pulsed applied voltage and the resulting capacitance transient 52

3-9. Circuit diagram for the pulsed isothermal transient capacitance measurement 54

3-10. Oscilloscope traces of the gate pulse, the ungated capacitance transient, and the gated capacitance transient 55

3-11. Oscilloscope traces of a single-gated capacitance transient and the gated capacitance transient averaged 2000 times 57

3-12. Oscilloscope trace of the calculated emission rate determined from eq (3-23) 58

3-13. Schematic C^{-2} versus V curves with defect centers uncharged and charged 61

3-14. Defect density N_t and dopant density N_d profiles 63

3-15. Thermally stimulated capacitance and current response of the midgap gold acceptor 65

3-16. Wafer maps of the gold acceptor defect density and the reverse leakage current 66

3-17. Plot of the reverse leakage current versus the acceptor defect density 67

4-1a. Spreading resistance uniformity across the diameter of an approximately 60-Ω·cm NTD silicon slice 71

Page

4-1b. Spreading resistance uniformity across the diameter of an approximately 60-Ω·cm standard float-zoned silicon slice 72

4-2. Spreading resistance profile of thyristor structure from cathode emitter side 73

LIST OF TABLES

2-1. Procedure for the van der Pauw Measurement 13

2-2. Summary of Theoretical Results 22

2-3. Representative List of Slices Measured 22

3-1. Mesa Fabrication Techniques 32

3-2. Junction Passivation Techniques 32

3-3. Structure Identification for NBS-13 33

PREFACE

This work was conducted as a part of the Semiconductor Technology Program of the National Bureau of Standards (NBS). This program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems of the Department of Energy (DOE) under DOE Task Order A021-EES Amendment No. 2. The contract is monitored by Mr. Jitendra P. Vora of DOE. The NBS point of contact for information on the various task elements of this project is F. F. Oettinger of the Electron Devices Division at the National Bureau of Standards. The work reported herein also drew upon the results of studies carried out under other parts of the Semiconductor Technology Program which were funded by the Defense Advanced Research Projects Agency under Order No. 2397, Program Code 7D10, and by the NBS.

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Measurement Techniques for High Power Semiconductor Materials and Devices

ANNUAL REPORT
January 1 to December 31, 1977

F. F. Oettinger, Editor

EXECUTIVE SUMMARY

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from the rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes. Application of this measurement technology will, for example, enable industry to make devices with higher individual power handling capabilities, thus permitting very large reductions in the cost of power handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon slices, (2) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime controlling or leakage source defects in power grade silicon material and devices, and (3) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

Photovoltaic Technique — One of the principal characteristics specified in the procurement of silicon for high-power devices is the radial variation of resistivity. These variations result from an inhomogeneous doping density. When fabricating high-power devices, both the solid-state diffusion and alloying steps are affected by the presence of variations in the doping density. Because of this, poor junction geometry and nonuniform current distributions are frequent problems in devices fabricated from inhomogeneous material. Device failures due to hot spots or thermal runaway may result. Gross variations in resistivity also cause wide variations in device characteristics and contribute to poor device yields. As an example, a localized low-resistivity region of a slice limits the

operating voltages of a device fabricated from that slice to a value lower than that expected from the remainder of the slice.

In the photovoltaic technique, a light spot is scanned along a slice diameter. The photovoltage and photoinduced change in specimen resistance are measured as a function of position along the slice diameter. From these two measurements, the variation in resistivity along the diameter can be computed. The technique requires no contact upon the slice surface area where a finished device or devices are to be fabricated. Thus, unlike the presently used methods for determining the resistivity gradients of silicon slices, this technique is nondestructive.

During this reporting period, the design, construction, and evaluation of a prototype automated measuring system capable of displaying the resistivity profile along two perpendicular diameters of large-diameter, high-resistivity silicon slices were completed. The system consists of a specimen translation/rotation stage, a laser light source, electronic measurement instrumentation, stage driver supplies, and a calculator-based controller which is programmed to perform all the experimental and analytical manipulations. Theoretical analyses have been performed to model various geometries (probe position, scanning position) which can be used with the photovoltaic measurement and to evaluate the effect of resistivity gradients perpendicular to the measurement scan. The system is currently capable of measuring the resistivity profile of float-zoned silicon of resistivity, $\rho \geq 50\ \Omega\cdot cm$, along a 51-mm slice diameter in about 2 min. Profiles so obtained are in substantial agreement with profiles obtained by four-probe measurements.

During the course of the work on characterizing the photovoltaic system, neutron transmutation doped (NTD) silicon became generally available. To see if the photovoltaic technique could be extended for use on this class of material, photovoltaic resistivity measurements were made on several specimens of NTD silicon. Because of the low-resistivity gradients and the low lifetime usually present in this material, the bulk photovoltage has been extremely small: less than 0.01 μV. In addition, the presence of a front-to-back surface photovoltage interferes with the bulk photovoltage to such an extent that meaningful measurements on NTD material have not usually been possible. The front-to-back surface photovoltage is present on all specimens, but is only a problem when it is of the same order of magnitude as the bulk photovoltage. This has been observed to be the case only in NTD silicon. Potential solutions to this problem have been identified but are not recommended for implementation until the need for profiling NTD silicon is established.

Deep Level Measurements — Measurement techniques are necessary for the detection and identification of deep level defects which affect the operation of power devices. Unintentional defects, which could be native to the starting material or introduced during wafer processing, can reduce carrier lifetime or contribute to leakage currents. Intentionally introduced defects are used to control the carrier lifetime and to tailor the switching characteristics of power devices. The ability to detect both intentional and unintentional defects for diagnostic purposes would greatly enhance the manufacturer's capability to control the quality (yield, reliability, and cost) of his product.

The utility of deep level measurement techniques for application to the design and fabrication of thyristors depends on the satisfaction of three major requirements: (1) routine test structure fabrication, (2) well-developed measurement methods, and (3) correlation of deep level defects with electrical device parameters. During this reporting period each of these areas was addressed.

In the area of test structure fabrication, the major accomplishment was the design and procurement of the mask set for test pattern NBS-13. This is a multilevel mask set specifically designed for the fabrication of mesa diodes on diffused thyristor slices taken from various steps in the manufacturing sequence. The following test structures are included on the pattern: mesa diodes of various sizes and geometries, MOS capacitors, etch rate monitors, metal continuity testers, contact resistors, and an alignment marker. Although a minimum of three levels is required, the mask set was designed with additional levels to allow maximum flexibility in order to optimize the mesa fabrication procedures. The mask set was used to fabricate mesa diodes by plasma etching; a reasonable yield of devices which would be satisfactory for deep level measurements was obtained.

In the area of measurement methods a number of subjects were investigated. Techniques were formalized for the analysis of isothermal transient capacitance data to yield energy levels and emission rates for both midgap and non-midgap defect levels. For midgap levels where majority and minority carrier emission rates could be approximately equal, a method was developed to allow separation of these rates for a more complete description of the defect level. The feasibility of using deep level measurement techniques for obtaining defect and lifetime profiles which are important in the model calculations of device behavior was investigated and demonstrated. Finally, a transient capacitance technique utilizing a repetitive series of charging pulses was established; this technique extends the measurable emission rates to times shorter than those obtained by present methods.

Correlation of deep level defects to measurable device parameters was investigated by measuring the leakage current of devices. For devices doped with gold, a definite relationship between reverse leakage current and defect density was obtained. This relationship was observable in wafer maps of gold defect density and leakage current.

Spreading Resistance Measurements — The ability to measure and control dopant profiles in various parts of thyristor structures is important for a variety of reasons. In thyristor substrate material, lateral uniformity of dopant, or lack thereof, strongly affects the reverse blocking voltage which can be achieved. In the fabricated thyristor, the surface concentration of the emitter layers; the shapes of the cathode emitter and of the *p*-base layer near their junctions with *p*-base and *n*-base, respectively; and the *n*-base resistivity are important features for process control purposes. In addition, such other features as the integral of the dopant density and of its first moment on both sides of the *p*-base to *n*-base junction are important for modeling and analysis of thyristor properties.

Spreading resistance measurements allow high spatial resolution for both lateral and depth profiling and large dynamic range for depth profiling of resistivity or carrier concentration in semiconductor structures. As such, this technique offers the possibility of process control on a routine basis if data can be made fully reliable and repeatable and if turnaround times and costs are acceptable. It also offers an essential complement to test structures for investigative troubleshooting in cases of yield loss or performance degradation. In addition, acquisition for the design or process engineer of data regarding the dopant profiles achieved by new or modified process steps is an important application. These data are needed both to close the design feedback loop and to assist in achieving reproducibility while establishing a process.

However, spreading resistance measurements must be calibrated against homogeneous specimens of known resistivity. This calibration is known to depend on conductivity type, on the surface preparation given to the specimen, and possibly on the dopant species. A known problem of nonstable or nonrepeatable response resulting from commonly used surface preparations is generally encountered in the *n*-base region both during incoming inspection of the starting material and profiling of finished device structures. Such instability results in inability to tighten design windows and in a widening of tolerances in process control. A second problem is possible inaccuracy in measuring *p*-base and anode-emitter profiles which results from the customary use of boron-doped silicon, because of its ready availability, for the calibration of systems used to measure gallium- and aluminum-doped diffused layers.

A task was undertaken at the beginning of FY 1978 to increase the reliability with which spreading resistance measurements can be used for radial resistivity screening of thyristor substrate material and for depth resistivity profiling of partially or fully fabricated thyristor structures. Emphasis is on the determination of procedures for the preparation of stable surfaces on high-resistivity, float-zoned, and NTD silicon. The following specific sub-task areas are included: (1) develop surface preparation procedures to permit stable and measurements on high-resistivity *n*-type silicon, (2) examine suitability of these surface preparation procedures for use on layer profiles, and (3) determine if the calibration of spreading resistance obtained from boron-doped specimens can be validly applied to measurements of thyristors fabricated with other *p*-type dopants.

1. INTRODUCTION

This project is directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes.

The project is designed to provide, disseminate, and foster the standardization of improved measurement methods required in high power semiconductor technology, for use in specifying materials and devices in commerce, and, by industry, in controlling device manufacturing processes and in designing systems. Application of this measurement technology will, for example, enable industry to: (1) make power semiconductor devices with greater uniformity of characteristics, thus permitting improvements in parallel and series connections of devices for applications from fusion generation to ac/dc conversion, (2) make devices with higher individual power handling capabilities, thus permitting large reductions in the cost of power handling equipment and fostering the development of dc transmission lines to reduce both energy waste and the extent of required rights-of-way, and (3) provide devices, and the systems utilizing them, with the reliability and performance required in energy generation, utilization, and conservation.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon slices, (2) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime controlling or leakage source defects in power grade silicon material and devices, and (3) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

2. PHOTOVOLTAIC TECHNIQUE

by

D. L. Blackburn
G. J. Rogers, and
R. D. Larrabee

2.1 Objectives

The overall objective of this task is to evaluate the feasibility of the photovoltaic method [2-1,2-2] as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon slices. In the photovoltaic technique, a light spot is scanned along a slice diameter. The photovoltage and photoinduced change in specimen resistance are measured as a function of position along the slice diameter. From these two measurements, the variation in resistivity along the diameter can be computed. Phase 1 of the task, January 1, 1976 to October 1, 1976, had the following objectives:

1.1 Develop a suitable system for making contact to the edge of the circular silicon slice; a key to this objective is the development of a system that provides good mechanical alignment of the contacts and a means for making improved nonrectifying contacts to the slice edge.

1.2 Design and construct a prototype automated measuring system capable of displaying or printing out the resistivity profile along two perpendicular diameters of large-diameter, high-resistivity silicon slices.

Phase 2 of the task, October 1, 1976 to October 1, 1977, had the following objectives:

2.1 Characterize the automated photovoltaic system for measuring resistivity uniformity of high-resistivity, large-diameter silicon slices.

2.2 Document the automated photovoltaic system for measuring resistivity uniformity of high-resistivity, large-diameter silicon slices; this objective involves the writing of a manual detailing the operation and construction of the system.

The annual report for the year 1976 (January 1, 1976 to December 31, 1976) [2-3] discussed the completion of Objectives 1.1 and 1.2. The present report discusses the completion of Objectives 2.1 and 2.2 and describes additional refinements to the system itself and solutions of several problems encountered during the first phase. A separate final report, in fulfillment of Objective 2.2, is being prepared for publication as an NBS Special Publication.

2.2 Background

2.2.1 Importance of Resistivity and Resistivity Variation for Power Devices

One of the principal characteristics specified in the procurement of silicon for high-power devices is the radial variation of resistivity. These variations result from an inhomogeneous doping density. When fabricating high-power devices, both the solid-state diffusion and alloying steps are affected by the presence of variations in the doping density. Because of this, poor junction geometry and nonuniform current distributions are frequent problems in devices fabricated from inhomogeneous material. Device failures due to hot spots or thermal runaway may result.

Gross variations in resistivity also cause wide variations in device characteristics and contribute to poor device yields. As an example, a localized low-resistivity region of a wafer limits the operating voltage of a device fabricated from that wafer to a value lower than that expected from the remainder of the wafer.

2.2.2 Limitations of Present Method

The method commonly used for determining the resistivity variation of starting wafers is the four-probe technique [2-4]. There are several difficulties with this method. A basic limitation in the application of the four-probe method to the measurement of resistivity variations is the relatively large sampling region of the probes [2-5]. Because of this, it has even been recommended that to obtain better spatial resolution, a two-probe measurement be made along a narrow bar cut from along the diameter of interest [2-6]. Also, there can be large errors introduced into the four-probe measurement due to slight mislocations of the probes [2-5,2-8]. An alternative probing method, the spreading resistance technique [2-7], has none of these difficulties, but it can be very slow and time-consuming. Perhaps the greatest limitation of any probing method is the requirement that probes be placed onto the slice surface in precisely those areas where diffusions and other processing steps are to occur. The damage caused by the probes may of itself be detrimental to the reliability and yield of devices fabricated in these slices. In addition, the method is very time-consuming when used to obtain the variations in resistivity over an entire slice diameter.

2.2.3 Photovoltaic Technique

The photovoltaic technique offers a nondestructive alternative for the measurement of resistivity variations along the diameter of circular silicon slices. The technique, which is based upon the theory of Tauc [2-9], requires no contact upon the slice surface area where a finished device or devices are to be fabricated.

The validity of a modified theory for circular silicon slices using the photovoltaic technique was demonstrated several years ago [2-2], but

the feasibility of this method for rapid automated measurement of high-resistivity, large-diameter slices remained to be demonstrated. It is the purpose of this task to determine this feasibility, and, if so determined, to fully develop a prototype system.

2.3 Review of Past Accomplishments

During 1976, two systems for making contact to the specimen were developed (Objective 1.1): one employing knife edges to contact the slice rim and the other, point probes to contact the top surface near the rim. Both systems adequately centered the slice for measurement.

The point probes were found to make more reproducible contacts and caused no damage to the slice edges due to chipping or cracking as the knife edges sometimes did. Further investigation of knife-edge contacts stopped, and all of the measurements discussed in this report were carried out with the point probes.

A prototype automated measurement system that is capable of measuring and displaying the resistivity profile along two perpendicular diameters of large-diameter, high-resistivity silicon slices was designed and constructed in 1976 (Objective 1.2). This system was further refined during the present reporting period.

During the early stages of evaluation of the measurement system (Objective 2.1), begun during 1976, a number of problems were identified. The major problems were the presence of a transverse photovoltage between the two contacts at the same end of a diameter and the inability to make reproducible measurements of the photoinduced change in specimen resistance. During this reporting period it was found that both problems were primarily a result of internal light scattering within the silicon slice as a result of using highly penetrating 1.15-μm wavelength radiation. Changing to highly absorbed 0.6328-μm wavelength radiation eliminated both problems.

2.4 Accomplishments This Year

During this year further refinements to the system were made to improve operations and solve problems encountered during the preliminary testing phase. A picture of the completed system is shown in figure 2-1 and a schematic in figure 2-2. A schematic of the computer-controlled measurement circuitry is shown in figure 2-3. The major additions to the system this year were:

1. The addition of a third digital input board to permit automatic readout of the value of the constant current source.
2. Changing the light source from the 1.15-μm wavelength helium-neon laser to the 0.6328-μm wavelength helium-neon laser.
3. The addition of pneumatic probe lowering systems to the specimen holder which permits the lowering of all four probe holders simultantously. A picture of the specimen holder with the

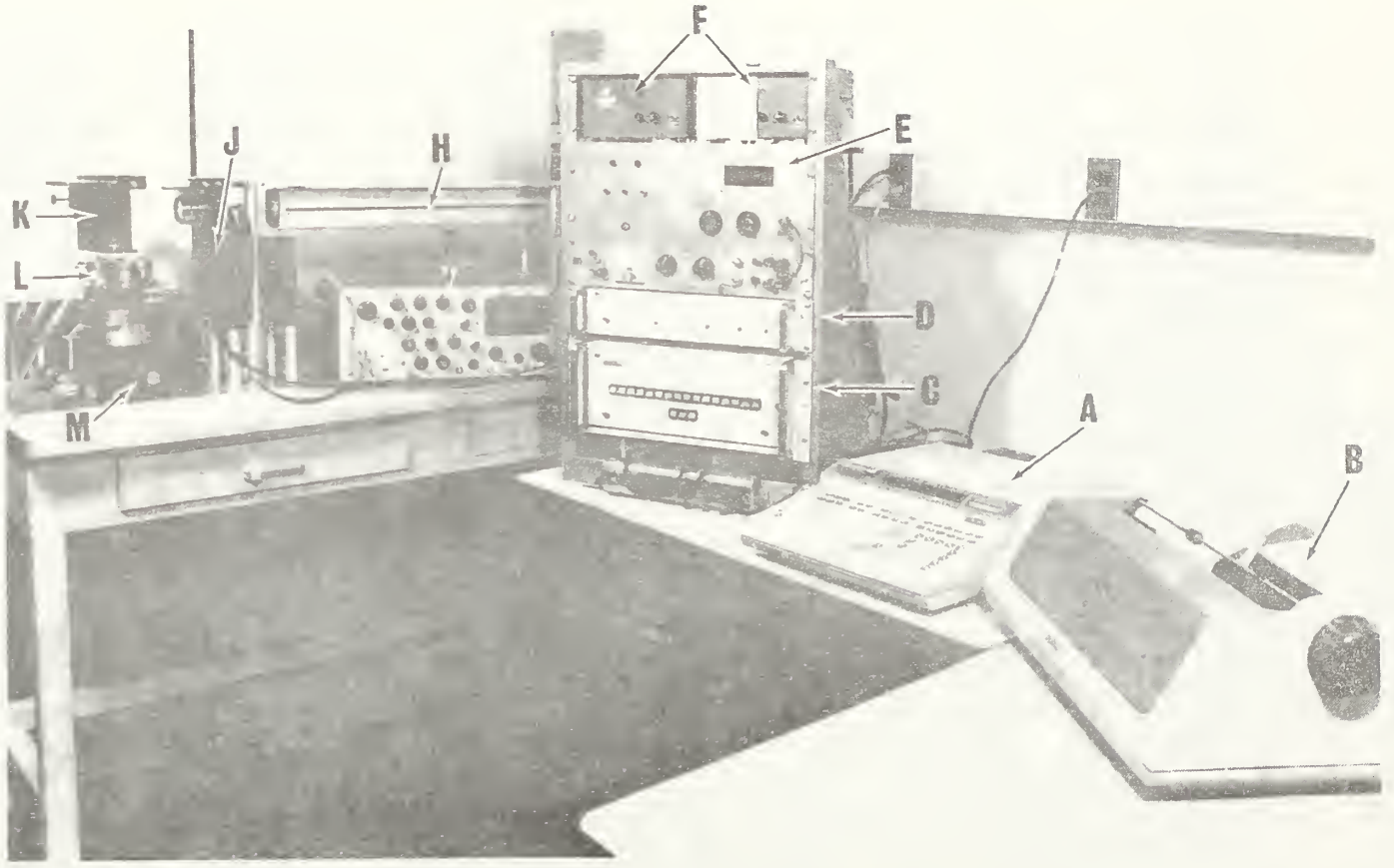
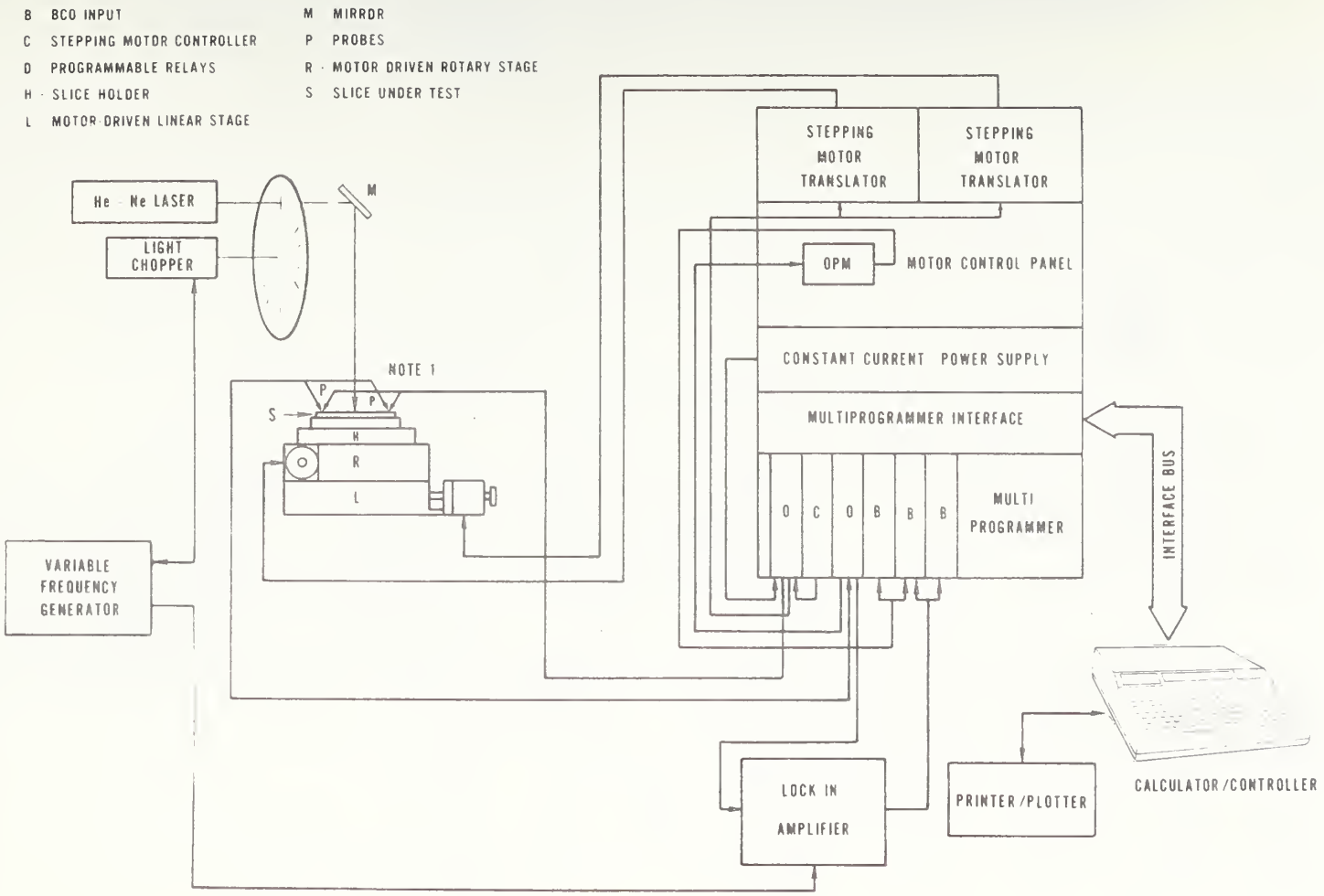


Figure 2-1. Photograph of automated photovoltaic resistivity gradient measurement system.

A - Calculator/Controller
B - Printer/Plotter
C - Multiprogrammer
D - Multiprogrammer Interface
E - Digital Panel Meter (DPM)
F - Stepping Motor Translators
G - Lock-in Amplifier
H - Helium-Neon Laser
J - Light Chopper
K - Mirror Assembly
L - Specimen Holder
M - Motor-Driven Stage



NOTE 1 THE PROBES ARE ACTUALLY PERPENDICULAR TO THE SURFACE OF THE SLICE UNDER TEST

Figure 2-2. Schematic of automated photovoltaic system.

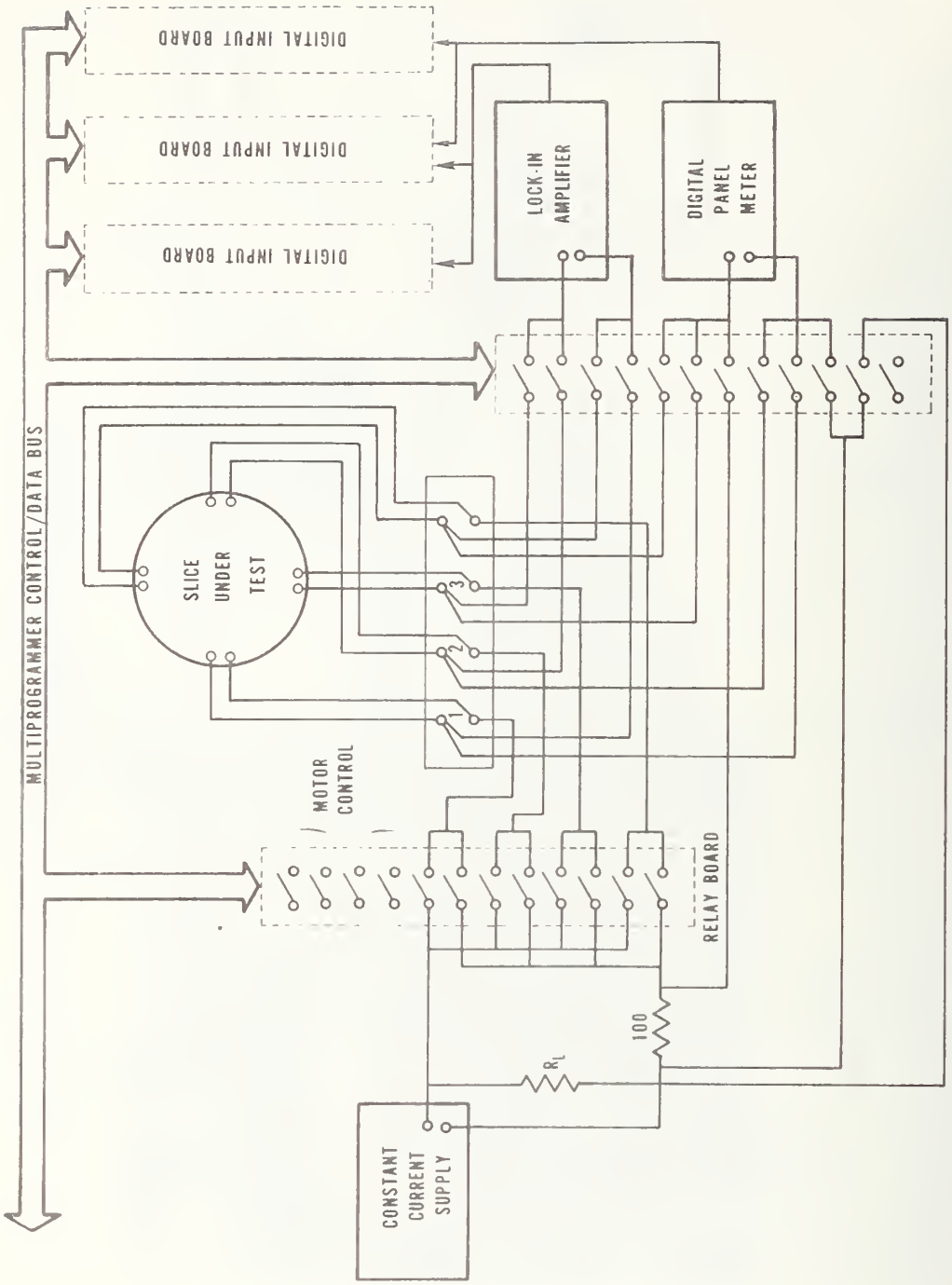


Figure 2-3. Schematic of computer-controlled measurement circuitry.

pneumatic system is shown in figure 2-4. A schematic of one of the pneumatic lowering systems is shown in figure 2-5; one system is needed for each probe holder.

4. The addition of relay boards to the multiprogrammer to permit automatic switching of current to the specimen for the photoinduced change in specimen resistance measurement and the van der Pauw average resistivity measurement. The average resistivity of the specimen can automatically be determined with the system by using the van der Pauw resistivity measurement procedure. To do this, the user places the specimen into the holder, lowers the probes, turns on the constant current source to the desired value (∿1 mA), types the specimen thickness into the computer, and instructs the computer (by pushing a button) to commence the measurement. The probe arrangement required for this measurement is shown in figure 2-6. The average specimen resistivity, $\bar{\rho}$, is determined from the expression:

$$\bar{\rho} = 1.1331\ t \left[\frac{V_{34} + V_{43}}{I_{21}} + \frac{V_{41} + V_{14}}{I_{23}} \right]$$

where t is the thickness and the other symbols are defined in table 2-1. Table 2-1 also lists the computer-controlled procedure for making the measurement.

Table 2-1 — Procedure for the van der Pauw Measurement

Constant Current Between Terminals	Step Number	Quantity Measured	Symbol
1+, 2-	1	Constant Current	I_{12}
1+, 2-	2	Voltage between terminals 3 and 4	V_{34}
1-, 2+	3	Constant Current	I_{21} (= I_{12})
1-, 2+	4	Voltage between terminals 3 and 4	V_{43}
2+, 3-	5	Constant Current	I_{23}
2+, 3-	6	Voltage between terminals 4 and 1	V_{41}
2-, 3+	7	Constant Current	I_{23} (= I_{32})
2-, 3+	8	Voltage between terminals 4 and 1	V_{14}

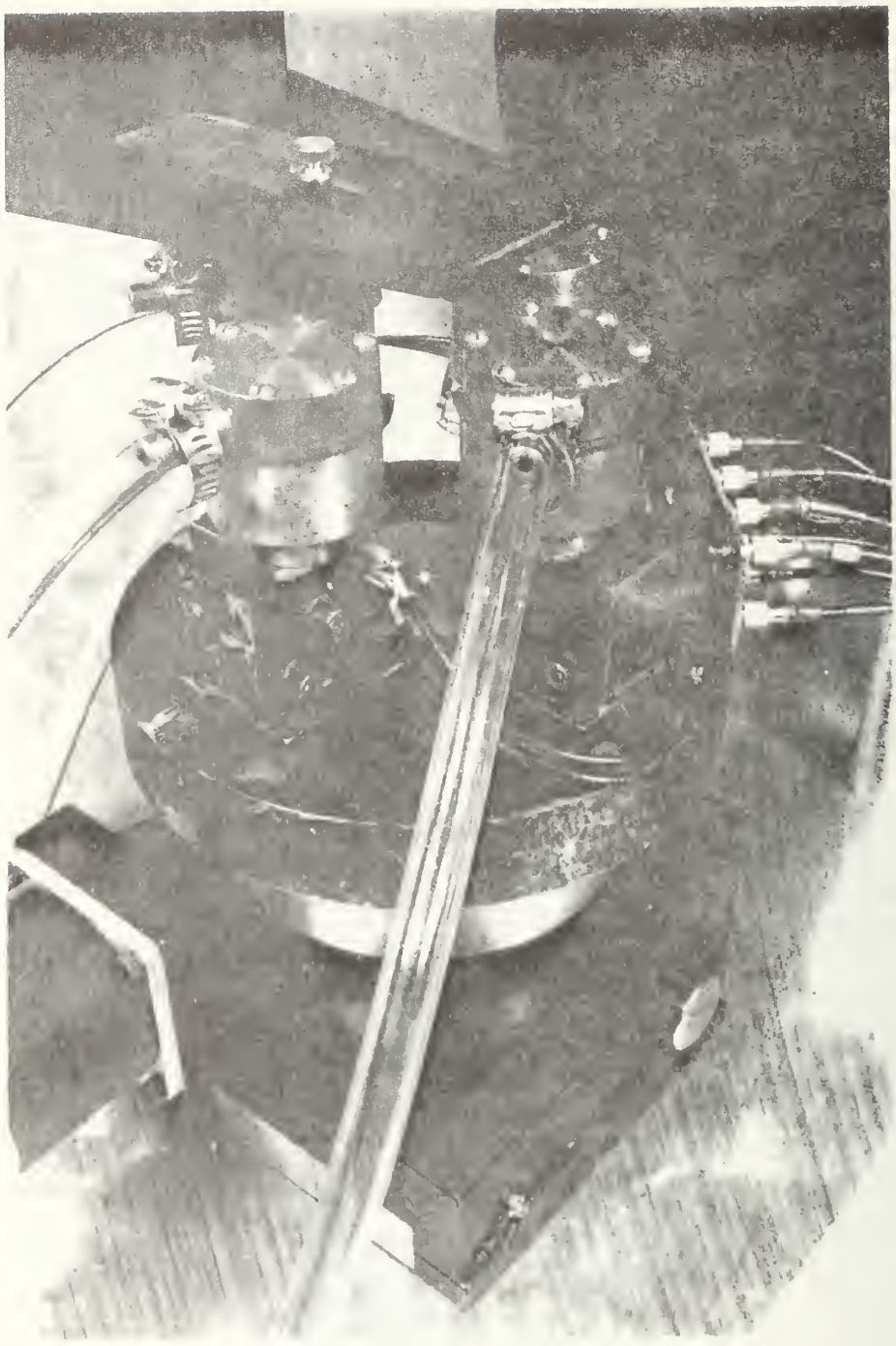


Figure 2-4. Photograph of specimen holder used with the photovoltaic system.

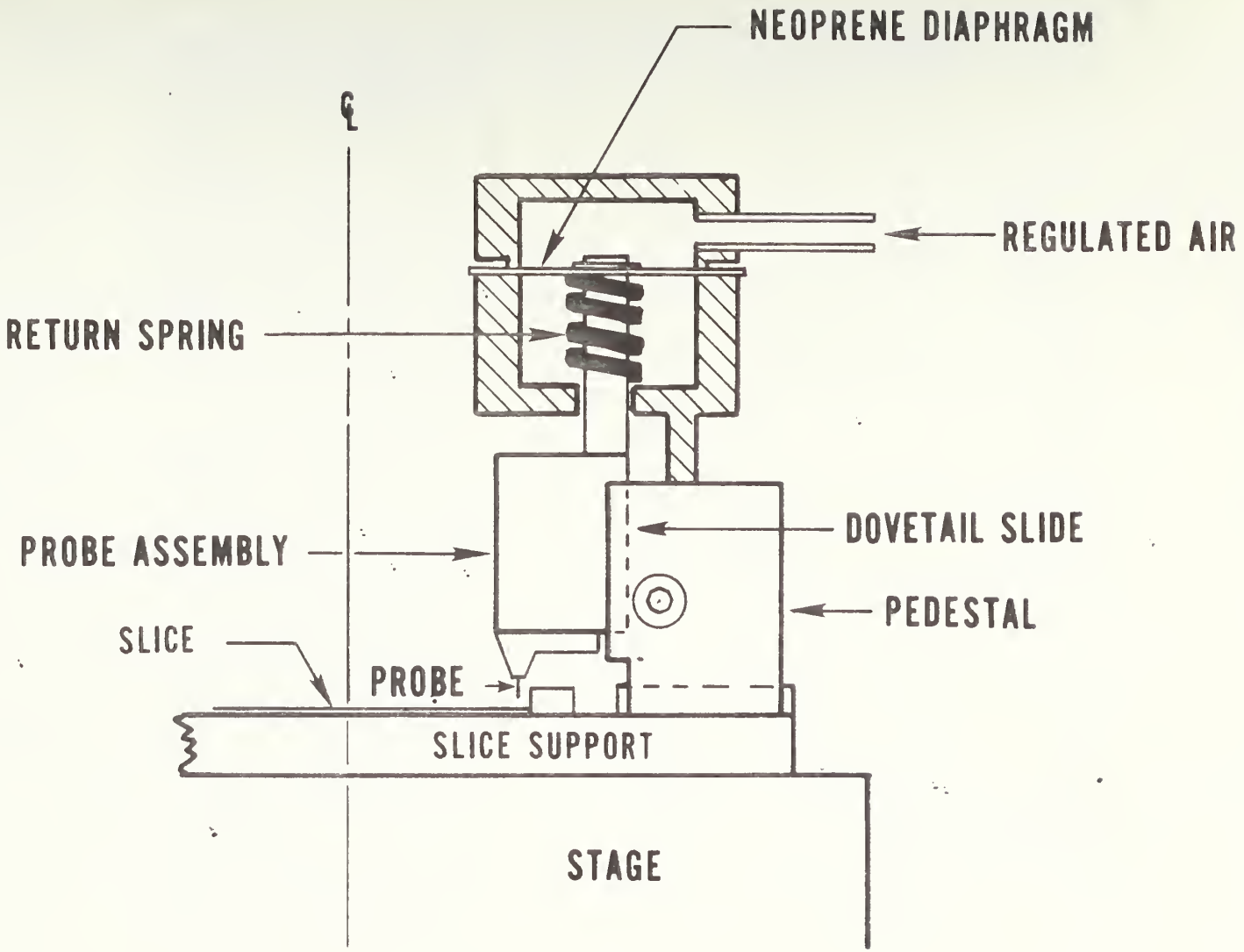


Figure 2-5. Schematic of one of the pneumatic probe-lowering systems.

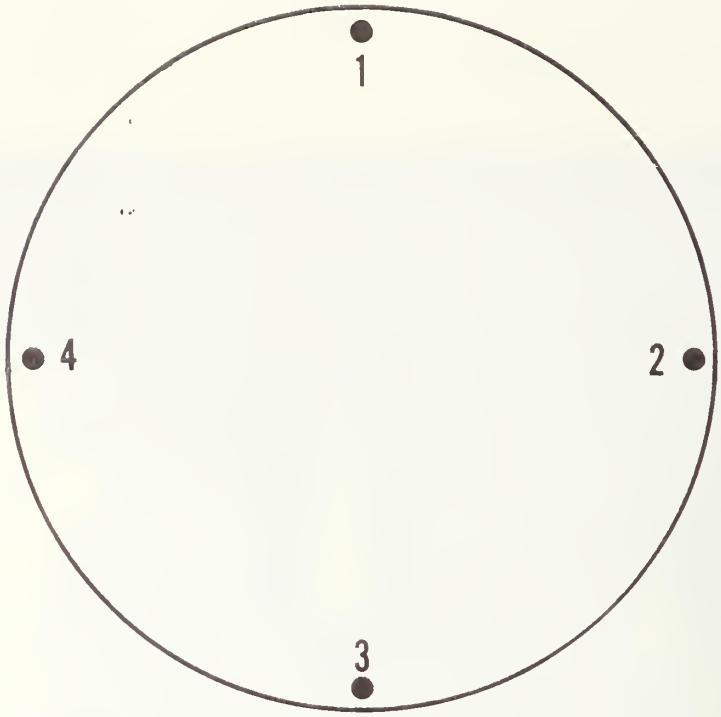


Figure 2-6. Slice geometry used for van der Pauw average resistivity measurement.

2.4.1 System Characterization (Objective 2.1)

Characterization of the automated system was completed this year. The major change which improved the operation of the system was the change from the 1.15-μm to 0.6328-μm wavelength radiation. It was also found that lapped slice surfaces yield the most reproducible results. The time required for measurement of a slice was established to be between 2 and 20 min, depending primarily upon the average specimen resistivity. In addition, a reworking of the mathematical analysis was done which yielded a more accurate expression for the resistivity gradient. Resistivity profiles as determined by the photovoltaic technique were compared with those measured by the four-probe method. The system was also used for preliminary measurements on neutron transmutation doped (NTD) silicon, and the problems to be expected in measuring such homogeneous, low-lifetime specimens were identified and some solutions proposed.

2.4.1.1 Illumination Wavelength

It was found that highly penetrating light, reflecting internally within the specimen, was the primary cause of the unwanted "lateral photovoltage" discussed in the previous report [2-3]. The light which scattered to the metal-semiconductor contacts at the diameter ends caused a metal-semiconductor barrier photovoltage to be generated there. For this reason, the laser wavelength was changed from 1.15 μm to 0.6328 μm. The

0.6328-μm radiation is absorbed very near the silicon surface. Because it does not deeply penetrate the silicon, it cannot scatter to the contacts. All of the photovoltaic resistivity gradient measurements discussed in the remainder of this report were made with the highly absorbed light.

2.4.1.2 Surface Finish

It was also found that the most reproducible results and the best agreement with four-probe measurement are obtained on slices for which both surfaces have been lapped with 12-μm alumina. Measurements on slices with polished surfaces have not been reproducible.

The reason for the differences between the results achieved on lapped and polished surfaces is not fully understood. Measurements show that a large surface photovoltage (comparable to or greater than the voltage between measurement contacts on the top surface) can be generated between the front and back surfaces if at least one of the surfaces is polished. Because of the lack of symmetry of the front-to-back-surface voltage with the measurement probes and because of the possible currents induced in the specimen by this voltage, the photovoltage measured at the contacts at the ends of the diameter can be affected.

The front-to-back-surface photovoltage may exist for specimens with both surfaces lapped, but its magnitude in this case is considerably less than the bulk photovoltage for most float-zoned specimens. Presently, all measurements are made on lapped surfaces. This probably is satisfactory for power grade silicon as the fabrication of devices does not require a polished starting slice.

2.4.1.3 Measurement Time

The total time for measurement depends upon the magnitude of the photovoltage signal and the magnitude of the photoinduced change in specimen resistance. The magnitude of the photovoltage depends upon the size of the resistivity gradient present (the larger the gradient, the larger the photovoltage) and the number of excess, steady-state electron-hole pairs (which is dependent upon the minority carrier lifetime and illumination intensity). For typical float-zoned material, both the resistivity gradient and the lifetime usually increase as the material resistivity increases. Similarly, the photoinduced change in specimen resistance is usually larger for high-resistivity material because this signal is proportional both to the lifetime and to the square of the resistivity. Because of the larger signals generated in higher resistivity float-zoned material, the lock-in amplifier integration time constant can be made smaller. In this work, for average resistivity, $\bar{\rho} \gtrsim 60$ Ω·cm, the time constant is usually set to about 100 ms. The light probe is made to remain at each measurement point for about 15 time constants (i.e., 1.5 s for $\bar{\rho} \gtrsim 60$ Ω·cm). Typically, 40 measurements are made for each scan along a diameter, so a total measurement time of 2 min is required for $\bar{\rho} \gtrsim 60$ Ω·cm (1 min for photovoltage, 1 min for photoinduced change in specimen resistance). The magnitude of the photovoltage for material

of this resistivity is usually less than 1.5 μV. For lower resistivity float-zoned specimens, $\bar{\rho} < 60$ Ω·cm, the photovoltage may be less than 0.01 μV in magnitude and the integration time constant of the lock-in is set to 300 ms or longer. The measurement time for this material usually ranges between 6 and 20 min.

*2.4.1.4 Theoretical Analysis**

The mathematical analysis of the photovoltaic problem on a circular specimen was reworked to extend the previous analysis. The new analysis was done more exactly and therefore is believed to be more accurate. The major conclusion from this effort was that all previously reported photovoltaic profiles should be multiplied by a factor of 4/3. The more exact analysis relates the gradient along a diameter to the photovoltage and photoinduced change in resistance measured at the ends of that diameter by the expression:

$$\frac{d\rho}{dx} = \frac{q}{\pi kT} \frac{[1 + (\mu_M/\mu_m)]}{1 - (x/b)^2} \frac{\bar{\rho}^2}{bt} \frac{V(x)}{\Delta R(x)} \qquad (2\text{-}1)$$

where

b = slice radius (cm),

x = distance of light spot from slice center (cm),

$\frac{d\rho}{dx}$ = resistivity gradient (Ω),

q = majority carrier charge (C),

K = Boltzmann's constant (J/K),

T = temperature (K),

μ_M = majority carrier mobility ($cm^2/V \cdot s$),

μ_m = minority carrier mobility ($cm^2/V \cdot s$),

$\bar{\rho}$ = average resistivity (Ω·cm),

t = thickness (cm),

$V(x)$ = photovoltage (V), and

$\Delta R(x)$ = photoinduced change in resistance (Ω).

The previous analysis of the photovoltaic portion of the photovoltaic technique [2-2] was extended in this work to include:

1. nonradial gradients in resistivity, and
2. arbitrarily positioned potential probes (i.e., probes placed anywhere on the slice surface).

*Principally funded by the Defense Advanced Research Projects Agency through ARPA Order 2397.

The photoinduced change in specimen resistance portion was worked out in detail only for a 0-deg and 45-deg positioning with respect to the measurement diameter.

The potential dipole created by a resistivity gradient in the illuminated spot region can be resolved into radial and azimuthal components. With respect to the specimen geometry illustrated in figure 2-7, these will be called U_x and U_y, respectively. In terms of the previous notation, the potential dipole $\langle U_\varepsilon \rangle$ had only an x component and corresponds to U_x of the present analysis. The potential at an arbitrary point P on the slice surface relative to the potential at point 1 at the end of the scanning diameter (see fig. 2-7), can be found by the method of conformal transformation in which the complex variable $z = x + iy$, describing the slice geometry (see fig. 2-7) is transformed into the variable $w = u + iv$ where:

$$w = \frac{1 - z/b}{1 + z/b} \tag{2-2}$$

with the following result:

$$V_{1P} = \frac{U_x}{b(1 + x/b)^2} \left[\frac{(u + u_0)}{(u + u_0)^2 + v_0^2} + \frac{(u - u_0)}{(u - u_0)^2 + v_0^2} \right] \tag{2-3}$$

$$- \frac{U_y}{b(1 + x/b)^2} \left[\frac{v_0}{(u + u_0)^2 + v_0^2} + \frac{v_0}{(u - u_0)^2 + v_0^2} \right] \tag{2-4}$$

where (see fig. 2-8):

$$u = \frac{1 - x/b}{1 + x/b} \tag{2-5}$$

$$u_0 = \frac{b - (x_p^2 + y_p^2)}{(b + x_p)^2 + y_p^2} \tag{2-6}$$

$$v = \frac{-2by_p}{(b + x_p)^2 + y_p^2} \quad . \tag{2-7}$$

The potential between two arbitrarily positioned potential probes P and P′ can be found by using eq (2-4) to find V_{1P} and $V_{1P'}$ and then using Kirchhoff's law:

$$V_{PP'} = V_{1P'} - V_{1P} \quad . \tag{2-8}$$

The special case of the potentials across the scanning diameter, V_{15} in figure 2-7, and the diameter perpendicular to this, V_{37}, are readily evaluated in this way and have relatively simple analytic forms:

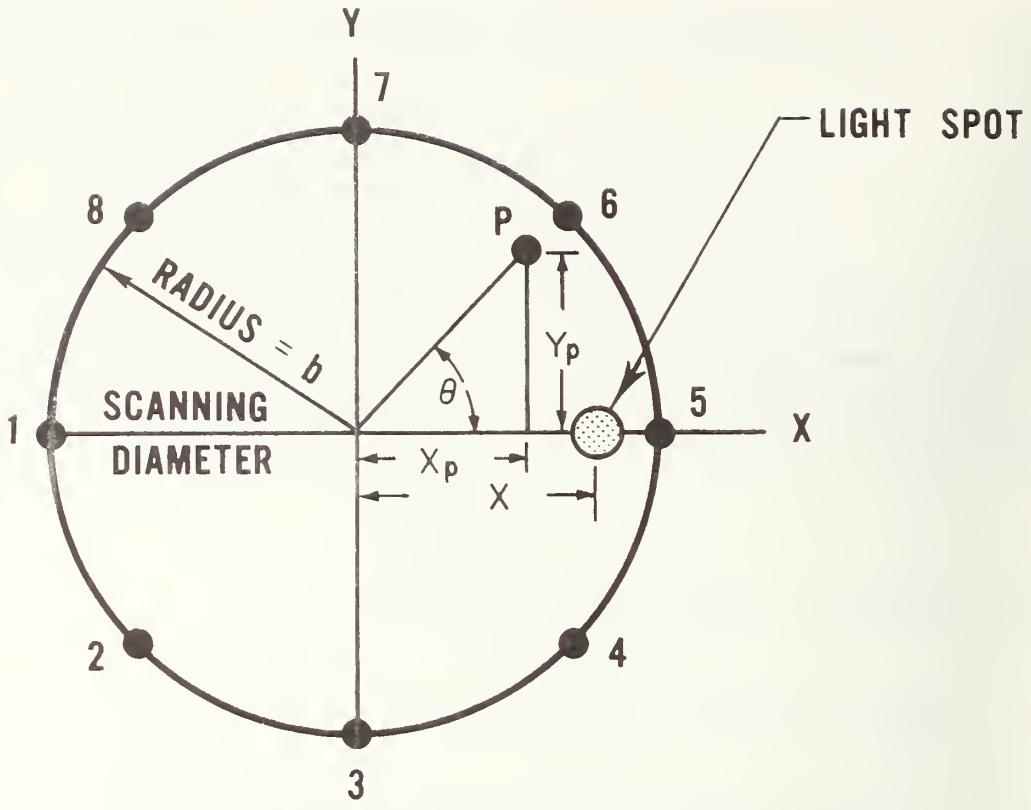


Figure 2-7. Geometry for theoretical calculations.

$$V_{15} = \frac{2U_x}{b(1 - x^2/b^2)} \tag{2-9}$$

$$V_{37} = \frac{4U_y}{b(1 - x/b)^2 \left(1 + \frac{(1 + x/b)^2}{(1 - x/b)^2}\right)} . \tag{2-10}$$

Equation (2-9) is identical in form to that obtained by the previous analysis [2-2] and is a function of U_x alone. However, the method by which U_x is evaluated differs in this work so that V_{15} is not identically equal to the previous result [2-2]. Equation (2-10) is a new result and shows that the voltage across the diameter perpendicular to the scanning direction is a function of U_y alone. Consequently, measurement of both of these voltages (i.e., V_{15} and V_{37}) allows one to measure both the radial and azimuthal components of the potential dipole in a relatively straightforward way.

Another potentially useful special case is concerned with the potentials across two perpendicular diameters oriented at 45 deg with respect to

the scanning diameter (i.e., V_{84} and V_{26} in fig. 2-7). The sum of these two voltages is a function of the radial component of dipole potential.

$$V_{84} + V_{26} = \frac{4U_x}{b(1 - x^2/b^2)} \left\{ \frac{1}{1 + \left(\frac{1 + x/b}{1 - x/b}\right)^2 (\sqrt{2} - 1)^2} - \frac{1}{1 + \left(\frac{1 + x/b}{1 - x/b}\right)^2 (\sqrt{2} + 1)^2} \right\} \quad (2\text{-}11)$$

and the difference is a function of the azimuthal component of the dipole potential:

$$V_{84} - V_{26} = \frac{-4U_y}{b(1 - x/b)^2} \left\{ \frac{(\sqrt{2} - 1)}{1 + \left(\frac{1 + x/b}{1 - x/b}\right)^2 (\sqrt{2} - 1)^2} + \frac{(\sqrt{2} + 1)}{1 + \left(\frac{1 + x/b}{1 - x/b}\right)^2 (\sqrt{2} + 1)^2} \right\} \quad (2\text{-}12)$$

This 45-deg probe arrangement is an attractive alternative to the present 90-deg arrangement because the light spot can be moved over the complete scanning diameter, yet not come close enough to a contact to produce extraneous effects due to photogenerated carriers reaching the metal-semiconductor contact.

This motivated an interest in looking at the analysis of the photoconductive portion of the present technique to see if it could also be solved for the 45-deg orientation geometry. In solving the photoconductive aspects of the problem, conformal mapping techniques were used twice in succession, once to handle the circular boundary of the wafer, and then a second time to handle the circular boundary of the small light spot. In each case the variable transformation of eq (2-2) was used. An image of the light spot is generated in solving the boundary conditions at the edge of the wafer in the first transform, and this image light spot must be included in the second transformation. This was ignored in the previous analysis because no way was found to evaluate its effects [2-2]. In the present analysis it was found that the image light spot is just as effective as the "real" light spot insofar as its effect on $\Delta R(x)$ is concerned. Therefore, its neglect led to an expression for $\Delta R(x)$ that was too small by a factor of two.

A second source of difference is concerned with the way the photovoltaic dipole moment of light spot was computed. Previously, an averaging over the circular light spot was used [2-2], whereas in the present case an approximate solution to the actual boundary value problem was obtained. The previous result was smaller than the present value by a factor of 2/3. The net effect of the factor of 2/3 in the photovoltaic term, $V(x)$, and the factor of 1/2 in the photoinduced change in specimen resistance term, $\Delta R(x)$, in the denominator, is a factor of 4/3 in resistivity gradient.

Table 2-2 summarizes the equations which have been derived for the four cases of current interest (i.e., measurement of the gradients of resistivity in the X- and Y-directions using either of the two geometries). The symmetry of these equations is quite interesting, although it should

Table 2-2. Summary of Theoretical Results

$$\text{Resistivity Gradient} = \frac{-C_1}{\pi(\frac{kT}{e})} \frac{(1 + \frac{\mu_{majority}}{\mu_{minority}})}{f(x)} \frac{\bar{\rho}^2}{wb} \frac{V(x)}{\Delta R(x)}$$

Parameter in Equation	Existing Geometry		45-deg Orientation Geometry	
	X-Gradient	Y-Gradient	X-Gradient	Y-Gradient
C_1	1	1	$1/2\sqrt{2}$	$1/2\sqrt{2}$
$f(x)$	$(1 - x^2/b^2)$	$(1 - x^2/b^2)^2/(1 + x^2/b^2)$	$(1 - x^2/b^2)$	$(1 + x^2/b^2)$
$V(x)$	$V_{51}(x)$	$V_{73}(x)$	$V_{62}(x) + V_{48}(x)$	$V_{62}(x) - V_{48}(x)$
$\Delta R(x)$	$\Delta V_{51}(x)/I_{51}$	$\Delta V_{51}(x)/I_{51}$	$\Delta V_{64}(x)/I_{82}$	$\Delta V_{64}(x)/I_{82}$

Table 2-3. Representative List of Slices Measured

Slice Identification	A Material Type	B ρ (van der Pauw) (Ω·cm)	C ρ_σ (Ω·cm)/%	D Correlation Coefficient*
45	FZ	151	12.89/8.5%	0.97
SP-10	FZ	10	0.72/7.2%	0.72
GND	NTD	104	0.66/0.6%	0.69
GNM	NTD	254	7.24/2.9%	0.85
24(B)	FZ	193	23.51/12.2%	0.85
42	FZ	173	16.96/9.8%	0.92
28	FZ	131	9.21/7.0%	0.93
26(B)	FZ	131	9.18/7.0%	0.86
27	FZ	163	10.8/6.2%	0.85
W2	FZ	60	5.99/10.0%	0.96
26	FZ	129	9.76/7.6%	0.94
4754	NTD	64	0.38/0.6%	0.51

*Represents 41 data points for each measurement technique.

be pointed out that V(x) and ΔR(x) have somewhat different definitions in the two geometries.

2.4.1.5 Experimental Results

Two examples of photovoltaic resistivity profiles on float-zoned silicon are shown in figures 2-8 and 2-9. For comparison, the four-probe profiles are also shown in the figures. A quantitative indication of the agreement can be seen in table 2-3, which lists a representative sampling of the slices measured in this study. The material is identified as either float-zoned (FZ) or NTD in column A and the average resistivity is given in column B. In column C is given the standard deviation, both absolutely and as a percentage of the average resistivity, of the four-probe measurements made along each diameter. This gives an indication of the variation in resistivity across the slice. In column D, the correlation coefficient between the four-probe and photovoltaic results is given for each slice for a least squares linear regression fit of the profile data. The data for the two slices of figures 2-8 and 2-9 are in the first two rows of the table.

These results demonstrate the suitability of the automated photovoltaic system for measuring float-zoned silicon with resistivity greater than 10 Ω·cm. The maximum resistivity float-zoned silicon measured in this work was about 200 Ω·cm for which good agreement with four-probe measurements was also achieved.

2.4.1.6 Extension to NTD Silicon

During the course of the work on characterizing the photovoltaic system, NTD silicon became generally available. To determine if the photovoltaic technique could be extended for use on this class of material, photovoltaic measurements were made on several specimens of this material. For most NTD specimens measured in this study, the resistivity variation as measured by the four-probe technique was very small (<5 to 10 percent). In addition, the minority carrier lifetime in NTD material is usually less than that in float-zoned silicon [2-10].*

The net result of the presence of the small resistivity gradients and the small minority carrier lifetime in NTD silicon is that the bulk photovoltage is very small. However, an anomalous photovoltage, which is larger than the bulk photovoltage expected to be generated by the gradients, is also present at the measurement contacts. This anomalous photovoltage does not appear to be associated with the resistivity gradient. The presence of this anomalous voltage makes accurate measurement of the resistivity gradient in NTD material impossible at this time for most specimens, as illustrated by the profiles shown in figure 2-10. The quantitative correlation is listed on row 3 of table 2-3. To date,

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* Measurements of lifetime were not within the scope of the project, but such measurements will be required to resolve fully the nature of the problems discussed here.

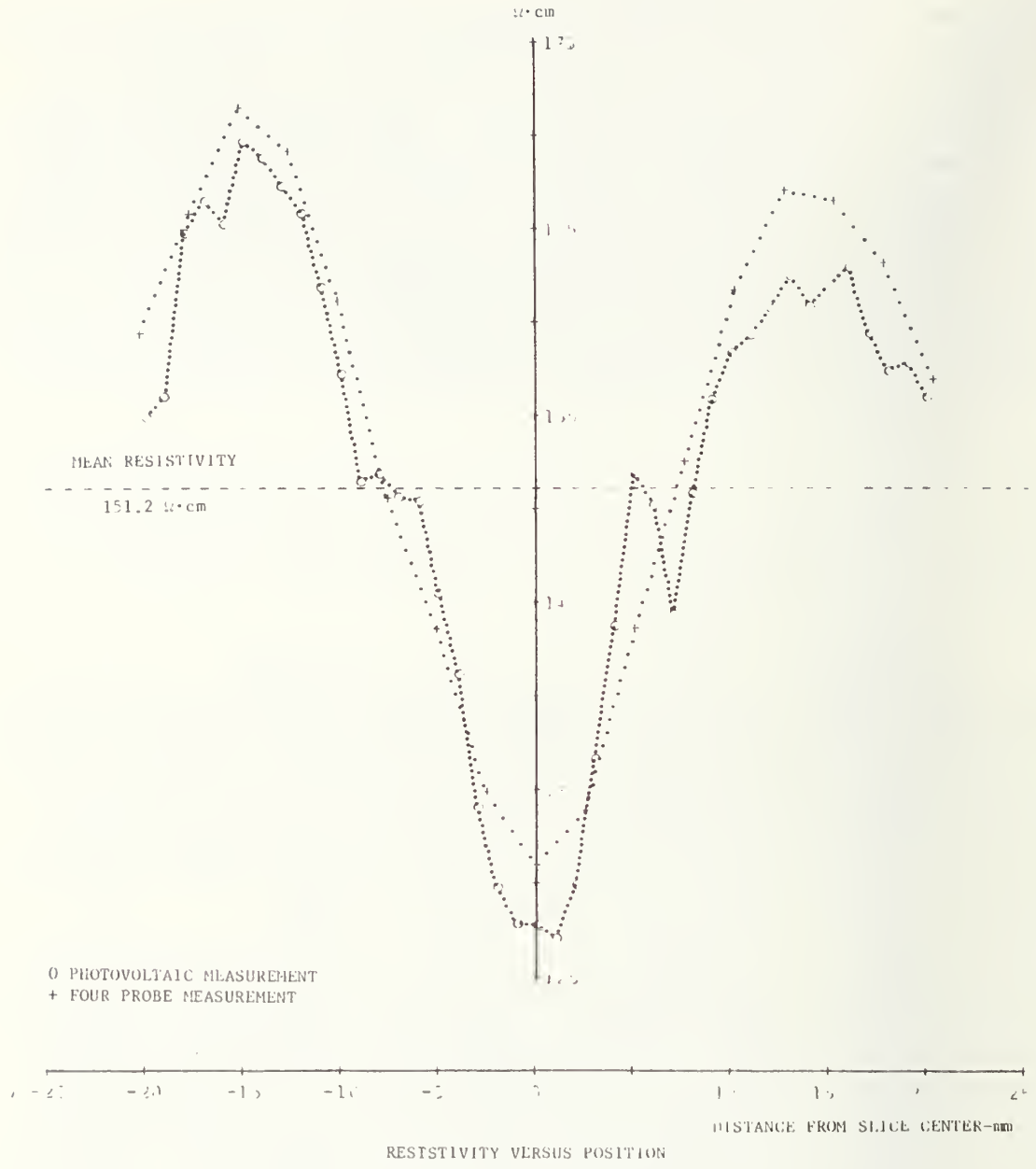

Figure 2-8. Comparison of four-probe and photovoltaic resistivity profiles for an *n*-type silicon slice of nominal resistivity of 150 Ω·cm.

Figure 2-9. Comparison of four-probe and photovoltaic resistivity profiles for an *n*-type silicon slice of nominal resistivity of 10 Ω·cm.

Figure 2-10. Comparison of four-probe and photovoltaic resistivity profiles for an NTD specimen with normal resistivity gradient.

the only NTD specimen for which good agreement between the photovoltaic and four-probe profiles has been obtained was one in which abnormally large resistivity gradients were present, as illustrated by the profiles shown in figure 2-11. The correlation data for these two profiles is listed in row 4 of the table.

The source of the anomalous photovoltage is not known. It may be associated with the front-to-back-surface photovoltage mentioned earlier in connection with measurements on polished float-zoned slices. The NTD slices were lapped on both surfaces, a condition for which the front--to-back-surface photovoltage does not cause a problem with float-zoned silicon. Because of the inherent uniformity of NTD silicon, a small anomalous voltage of the order of 0.02 μV would, in most instances, make accurate measurement of the NTD material impossible, but an anomalous voltage of this size would have little effect on the photovoltaic measurement of most float-zoned material.

If the anomalous voltage is a result of the front-to-back-surface photovoltage, there are at least three potential methods for eliminating the problem. One is to chemically treat the surfaces in some way so that the carrier density at both surfaces is always the same. This would not appear to be a very promising approach and would detract from the nondestructive nature of the measurement. Another method would be to place measurement probes on both the bottom and top surfaces. One should be able to eliminate the effect of a front-to-back-surface photovoltage by combining the measurements made between the proper combinations of probes on the back-to-top surfaces. A third, and perhaps most promising approach would be to illuminate the specimens simultaneously from both sides. The laser beam would be split and made to impinge as a spot from above and below the slice. This would tend to make the carrier densities the same at both surfaces. Another advantage is that for the 0.6328-μm radiation, the carrier density within the specimen beneath the light probe would be the more uniform, better satisfying one of the boundary conditions.

Further investigation of these potential solutions to overcoming the effects of the anomalous photovoltage is not recommended at this time. Because of the apparent uniformity of resistivity of NTD silicon, it is not clear that a point-by-point screening procedure would be justified. This conclusion will be reassessed as NTD silicon becomes more widely used.

2.4.2 Dissemination of Results (Objective 2.2)

The results of this effort have been disseminated through various means during the year. A discussion of the photovoltaic work was a major portion of a paper [2-11] presented by R. Y. Koyama of NBS at the Electric Power Research Institute Light Fired Thyristor Workshop held in Palo Alto, California, in October 1977. This material was also chosen to be published in the *NBS Journal of Research* [2-12]. The automated system was described to over 70 participants of a tour of the NBS Semiconductor

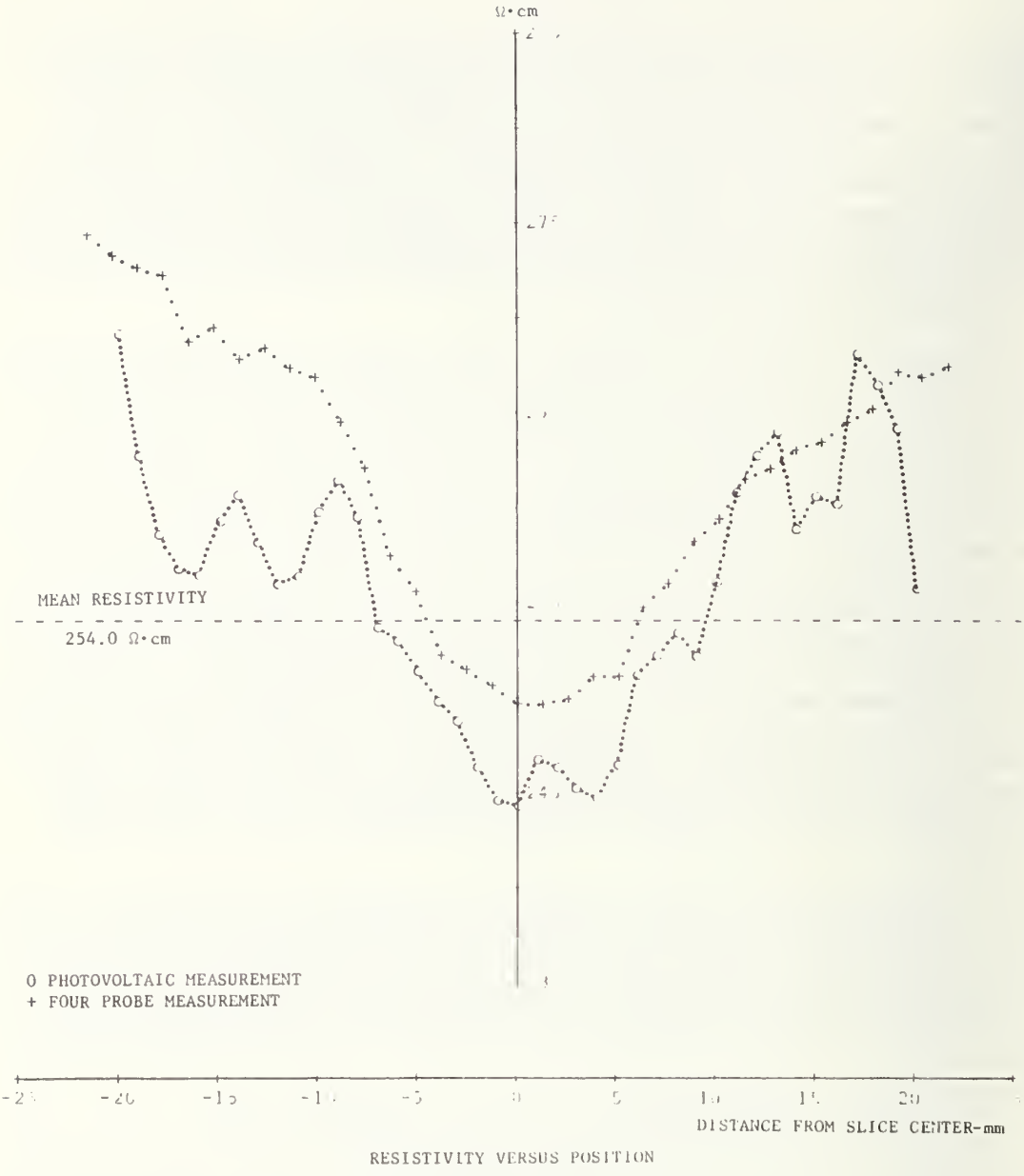

Figure 2-11. Comparison of four-probe and photovoltaic resistivity profiles for an NTD specimen with an abnormally large resistivity gradient.

Technology Program that was specially conducted for attendees of the December 1977 IEEE International Electron Devices Meeting.

A paper describing the automated system and improved theoretical analysis has been accepted by The Electrochemical Society for presentation at its Topical Conference on Characterization Techniques for Semiconductor Materials and Devices to be held in Seattle, Washington, in May 1978. Finally, a final report of the automated photovoltaic system, which will include detailed instructions for construction and operation of the system, is being prepared and will be issued as an NBS Special Publication.

3. DEEP LEVEL MEASUREMENTS

by

R. Y. Koyama J. Krawczyk
W. E. Phillips S. Y. Liu
D. R. Myers*

3.1 Objectives

The overall objective of this task is to evaluate the use of thermally stimulated current and capacitance measurements (TSM) and other deep level measurement techniques for characterizing defects which control leakage current and lifetime in power grade silicon materials and devices. Phase 1 of this continuing task was completed in October 1976. Phase 2 of this task, October 1976 to October 1977, had the following objectives:

2.1 Develop procedures for the fabrication of MOS capacitors and *pn*-junction structures on diffused power thyristor wafers taken from the process line to allow characterization of defects in processed material.

2.2 Utilize TSM to detect defects in processed power device material and examine various interferences which could obscure or distort the defect response.

2.3 Establish the transient capacitance technique as an adjunct to the conventional stimulated current and capacitance measurement and evaluate the feasibility of using deep level measurements for defect (lifetime) profiling.

Phase 3 of the task, October 1977 to October 1978, has the following objectives:

3.1 Complete the development of the fabrication procedures used to produce mesa diodes. These procedures are to be compatible with thyristor manufacturing procedures so that they can be used routinely to analyze and control manufacturing processes.

3.2 Establish routine procedures for utilizing TSM (dynathermal and isothermal) and analyzing TSM data with emphasis on investigation of the metrological aspects of the measurement method associated with midgap defect centers which control the carrier lifetime. Defects such as gold or platinum (common lifetime killers) or other purposely introduced defects will be used as study vehicles in establishing these procedures.

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* NBS-NRC Post-doctoral Fellow.

3.3 Develop capabilities to measure electrical parameters of devices (fabricated test structures such as *pn*-junctions and MOS capacitors, and commercial devices such as rectifiers and thyristors) so that the parameters can be related to the presence of defects.

This report discusses the progress that has been made in each of these objective areas during calendar year 1977.

3.2 Background

Deep level defect measurements such as TSM [3-1] and deep level transient spectroscopy (DLTS) [3-2] utilize the ability of active defects in depletion regions to trap carriers and to emit them after receiving sufficient thermal energy. Suitable analysis of the measured data allows determination of the density, energy level, and emission rate of the defect. The interest in measurement of deep levels in semiconductors, particularly in application to power devices, stems from two related aspects: 1) detection, identification, and control of unwanted intrinsic or process-induced impurities or defects, and 2) characterization and control of specifically introduced defects for lifetime control. These techniques, which have generally been confined to laboratory studies of packaged devices, have now been extended to measurements on devices in wafer form [3-3, pp. 26-46], and routine procedures for measurement and analysis of data have been established so that these techniques can be utilized as diagnostic tools in the fabrication area as well as in the research laboratory.

3.3 Accomplishments This Year

3.3.1 Test Structure Development (Objectives 2.1 and 3.1)

The useful and routine application of these deep level measurements to diffused power device wafers requires the development of procedures for the fabrication of test structures. The basic test structure is a diode which utilizes one of the two junctions that are deeply diffused during the first high temperature treatment of thyristor manufacture. Because both sides of these diodes are not accessible externally, methods are being developed to fabricate an array of mesa diodes in order to isolate a number of independent test devices on the wafer. Although the complete process could involve many individual steps, the general procedure includes, as a minimum, the following steps:

1) define mesa,

2) cut moat in the silicon to isolate devices,

3) provide junction passivation,

4) cut contact windows on the passivation layer, and

5) pattern metallization.

A mask is required to define the protected mesa areas (mask level 1) during the moat etch for junction isolation. Following the moat etch, some form of junction passivation to minimize surface leakage is necessary. Then contact windows (mask level 2) are opened to both the p^+ diffusion and the n-base of the wafer. Finally, the contact metallization is applied and defined (mask level 3). Hence, this process requires a minimum of three masking levels.

In terms of processing technology, the most difficult parts of the fabrication procedure are the mesa formation and the junction passivation steps. A variety of procedures have been considered. These are listed in tables 3-1 and 3-2.

Table 3-1

MESA FABRICATION TECHNIQUES

	Technique	Mask Material
1	Ultrasonic Machining	Tool Configuration
2	Plasma Etching	Photoresist
	and	CVD* Silicon Dioxide
	Chemical Etching	Thermal Silicon Dioxide
		Silicon Nitride
		Black Wax
		Metal Film
3	Mechanical Sawing	None

* Chemical Vapor Deposited

Table 3-2

JUNCTION PASSIVATION TECHNIQUES

1. CVD* Silicon Dioxide
2. Thermal Silicon Dioxide
3. Silicon Nitride
4. Silicone Rubber

* Chemical Vapor Deposited

A further consideration is the necessity to make good ohmic contact to both regions of interest. Although no problem is anticipated with metallization to the diffused p^+ region, contact to the high resistivity n-region could present problems.

During the first quarter of Phase II (October - December 1976) some successes were achieved using the ultrasonic machining and plasma etching techniques; these have already been reported [3-3, pp. 46-55]. Sample devices were fabricated by utilizing existing mask sets (NBS-2 [3-4], and a dot matrix) which had been designed for other processing techniques. Chemical etching procedures were not attempted due to anticipation of undercutting and liftoff of the mask material. Mechanical sawing also was not used due to lack of masks appropriate for cutting the contacts and patterning the metallization.

Table 3-3

STRUCTURE IDENTIFICATION FOR NBS-13

Structure Number	Identification
1	20-mil (508-μm) diameter mesa diode with gate
2	10-mil (254-μm) diameter mesa diode with gate
3	20-mil (508-μm) diameter mesa diode
4	20- by 20-mil (508- by 508-μm) square mesa diode with gate
5	10-mil (254-μm) diameter mesa diode
6	30-mil (762-μm) diameter mesa diode
7	60-mil (1524-μm) diameter mesa diode with gate
8	30-mil (762-μm) diameter mesa diode with gate
9	15-mil (381-μm) diameter MOS capacitor over p^+ with gate
10	15-mil (381-μm) diameter MOS capacitor over n with gate
11	etch monitor and metal continuity tester
12	etch monitor
13	metal to p^+ contact resistor
14	metal to silicon contact testers
15	alignment marker and level identification
16	mask identification

Because of the developmental nature of the fabrication procedures involved, a significant effort was aimed at the design and procurement of a mask set which would aid in the optimization of the fabrication procedures. Such a mask set should be flexible in its use with different procedures at different points in the process. It should also provide some diagnostics as well as anticipate some of the problems. The resulting mesa diode mask set, designated NBS-13, consists of eight separate levels, but all eight levels are not required for any process. There are eight mesa diodes of various sizes and configurations, two MOS capacitors, two etch monitors, several contact testers, and an alignment marker.

Figures 3-1a and 3-1b are photographs of the eight levels of NBS-13. The individual structures are numbered on level eight. Table 3-3 identifies each of the individual structures.

An example of the use of this mask set is illustrated in figure 3-2. Mask 1 is used to define the mesa areas. This is followed by passivation. Masks 5 and 6 are used to define the contact windows and the metallization to the n-regions. Masks 7 and 8 are used to define the contact windows and the metallization to the p^+ regions. The five-step process illustrated in figure 3-2 has a second alternative in the event of contact problems with the n-region. It would be possible, for diagnostic reasons, to include an n^+ diffusion after the n-contact cut (step 4) to compare the quality of this n-region contact with those lacking this diffusion. This is done with Mask 2 of NBS-13. A diffusion step is a high temperature process. Since it is possible that such high temperature treatments could alter the material under study, it is not a desirable procedure and probably will not be used with respect to TSM characterization of diffused power device wafers. However, this alternative provided by the mask set offers a powerful diagnostic tool in the development of a suitable fabrication procedure and was included for this reason.

Following design of NBS-13 and the procurement of the mask set late in 1977, some progress has been made in the study of fabrication procedures. Because chemical etching procedures are readily available in all semiconductor facilities, a mesa fabrication procedure utilizing chemical etching would be a desirable method. Several different masking techniques were investigated:

1. silk screened application of black wax,
2. black wax/photoresist,
3. evaporated metal films, and
4. multiple photoresist.

As anticipated, the major drawback to this method is undercutting and liftoff of the masking materials. However, the most successful technique among these was the multiple photoresist technique. This method utilizes the multiple application of a commercial photoresist of high solids content and viscosity. After each development step, the resist is baked for 20 min at 175°C to increase the durability during the mesa

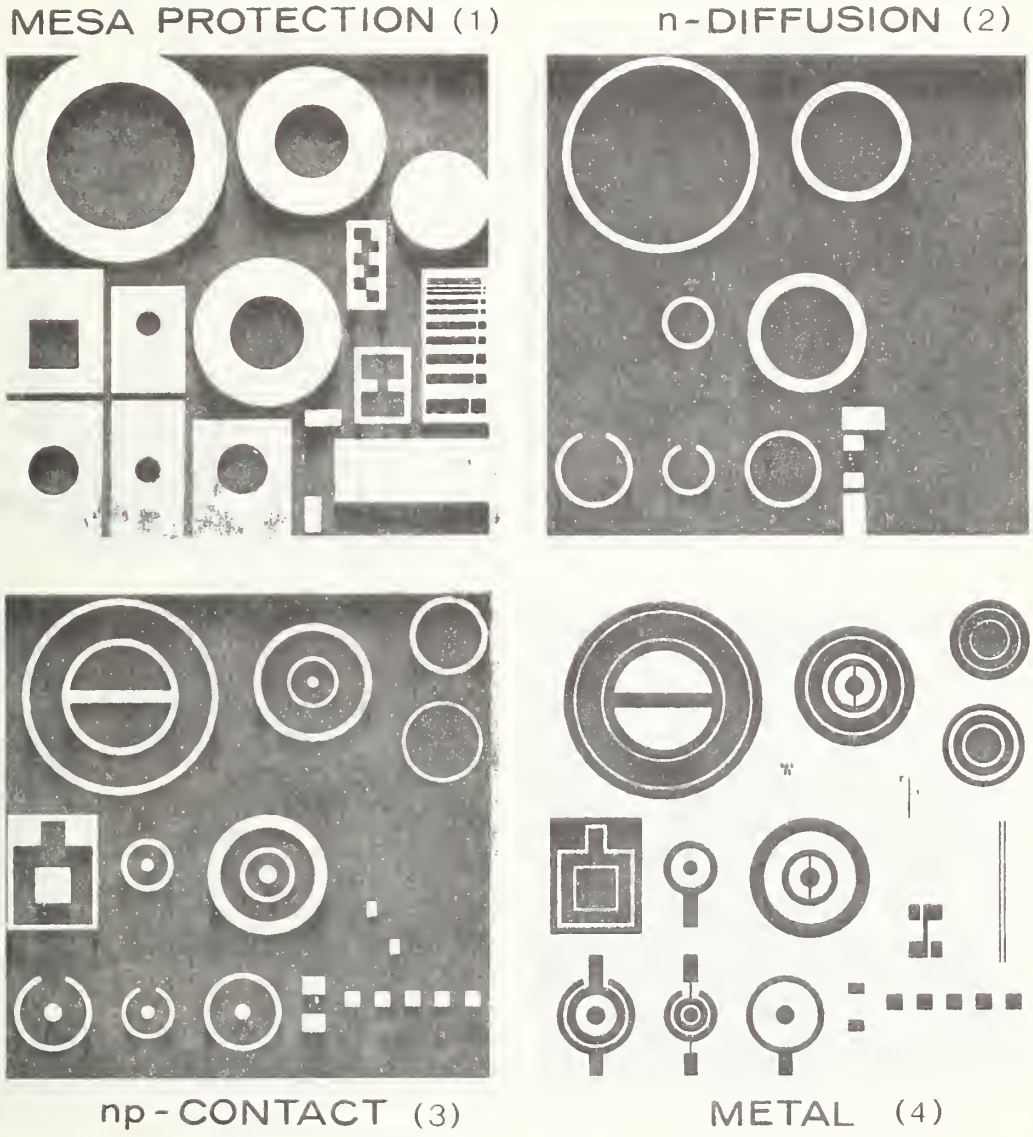

Figure 3-1a. Photographs of levels 1 through 4 of the NBS-13 mesa diode mask set.

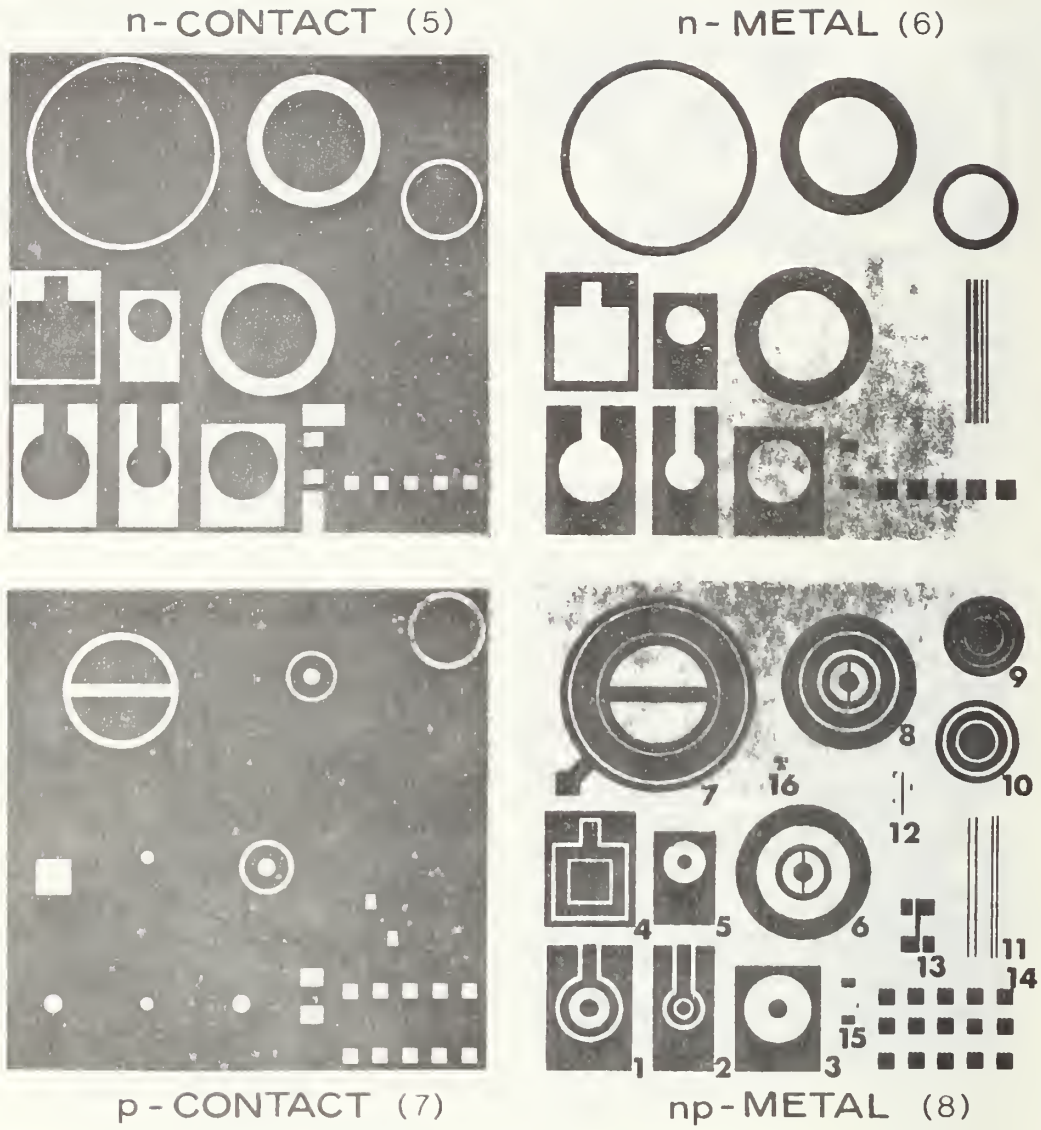

Figure 3-1b. Photographs of levels 5 through 8 of the NBS-13 mesa diode mask set. The structure numbers are given on level 8 and are identified in table 3-3.

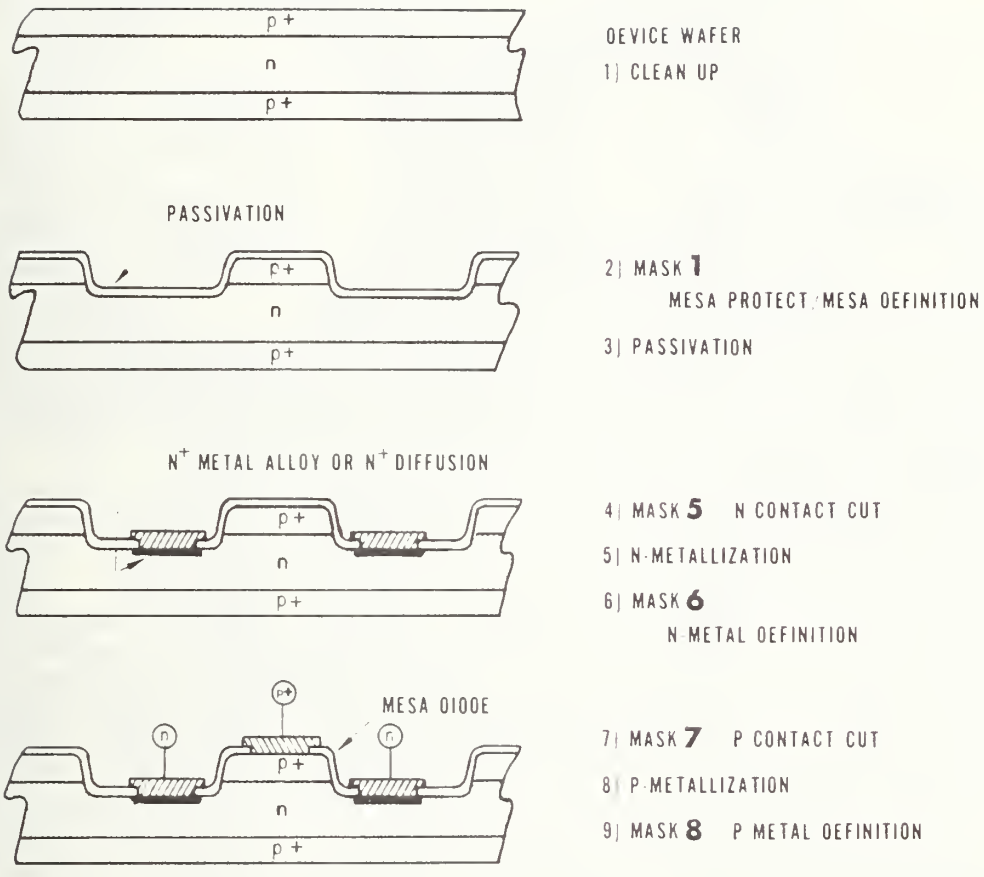

Figure 3-2. A mesa diode fabrication procedure using five mask levels to separate the n- and p^+-metallization steps.

etching step. By use of a planar etch consisting of 1 part hydrofluoric acid, three parts nitric acid, and three parts acetic acid, mesa structures as deep as 90 μm have been etched. Although undercutting of the resist is unavoidable, mesas have been fabricated with this method. The other techniques had limited success. The major difficulty was lack of adherence of the masking agent to the silicon wafer surface; in some cases the pin hole density in the mask material proved to be excessive for successful use.

The use of "dry" processing techniques, in particular, plasma etching and stripping, is becoming more prevalent and important in semiconductor processing. The use of plasma etching for mesa fabrication was considered to be excessively time-consuming [3-3, pp. 54-55]. It has been found, however, that if the etching is done with reduced loading of the machine (one or two wafers at a time), it is possible to achieve etch rates approaching 40 μm/h. Although this rate is considerably slower than other methods, it is usable. Figure 3-3 is a photomicrograph of one cell of a wafer on which the plasma etching technique was used to fabricate the mesa diodes. Only Mask Levels 1, 3, and 4 of NBS-13 were used. The mesas were etched on an n-type wafer which had been previously diffused with boron to a depth of approximately 0.5 μm. The mesas are about 12 μm deep and the masking agent was a combination of thermal oxide and photoresist. Also, since these were preliminary investigations for defining plasma etching procedures, thermal oxide was used for the passivation. The yield for low leakage devices (<50 nA, at room temperature) was about 40 percent for a sampling of the smaller devices (structures 3 and 5) that were measured. The 50-nA leakage level is satisfactory for deep level measurements (TSM). Forty percent is a reasonable yield to work with in terms of defect detection; however, detailed wafer mapping of defects would require yields with little or no bad devices in the central region of the wafer.

3.3.2 Utilization of Thermally Stimulated Measurements for the Detection of Defects (Objectives 2.2 and 3.2)

The effect of signals which could distort or mask the desired TSM signal was investigated during the period October - December 1976. Hence, this was reported in the last Annual Report [3-3, pp. 56-60]. Primary efforts during 1977 were concentrated on the development and analysis of routine measurement procedures. For this work silicon specimens with intentionally added sulfur were used. Sulfur was chosen because it has both a midgap and a shallow level and is easy to implant.

The following measurement procedures were developed: 1) thermally stimulated current and capacitance measurements which provide a quick identification of well-known defects and a measure of their density; 2) isothermal transient capacitance measurements which provide a precise measurement of the combined electron and hole emission rate from the defect center over a range of temperatures and from which the energy level(s) can be determined; 3) isothermal initial and final capacitance measurements which provide a ratio of the minority-to-majority-emission rates; and 4) isothermal capacitance-leakage current measurements which

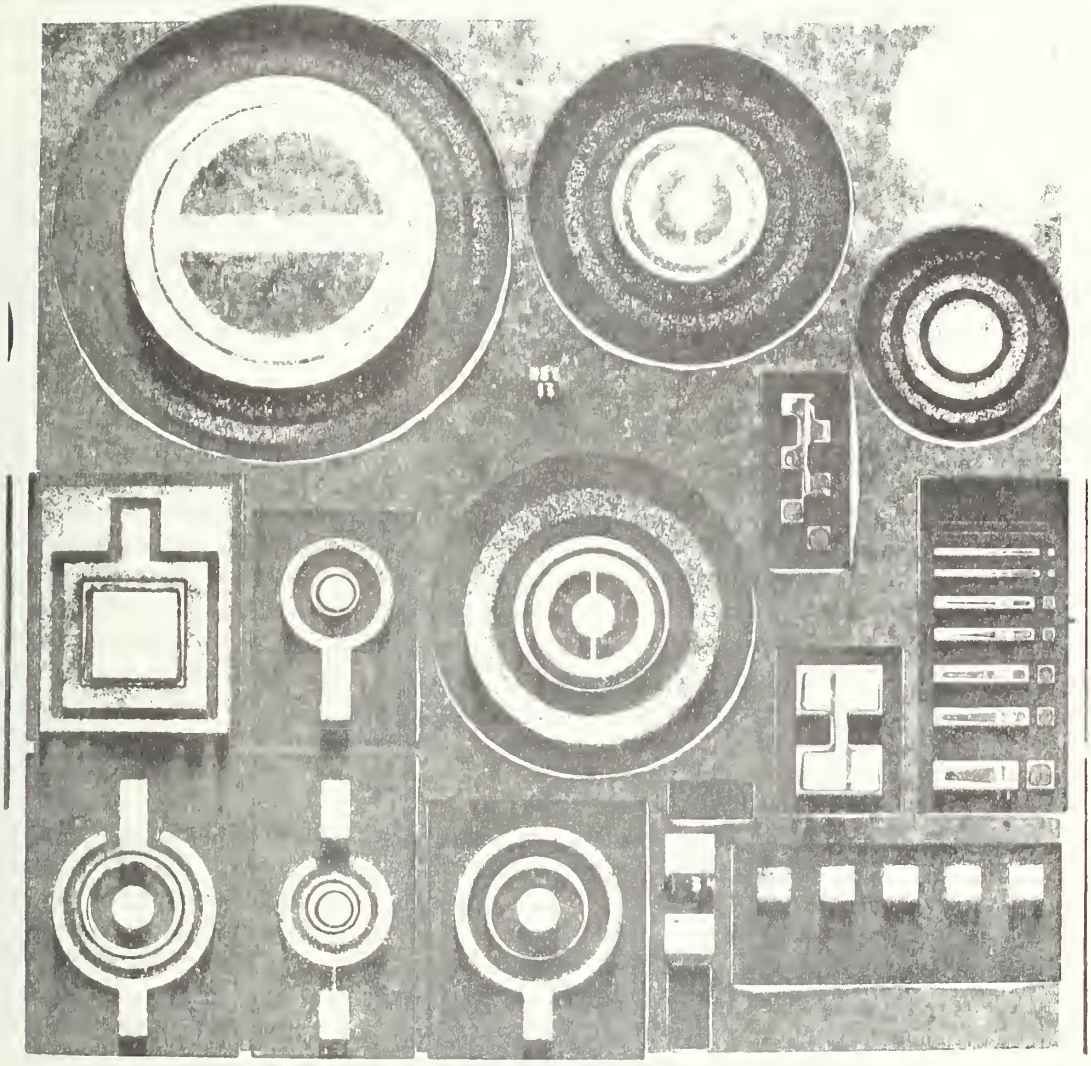

Figure 3-3. Photomicrograph of one cell of a plasma-etched wafer using the NBS-13 mask set. Only mask levels 1, 3, and 4 were used.

provide a different combination of majority and minority emission rates, namely, the ratio of their product to their sum. The first two procedures are described in section 3.3.2.1, and the last two procedures are described in section 3.3.2.2.

3.3.2.1 Analysis of Defect Levels

Thermally stimulated current and capacitance measurements were made on sulfur-implanted *n*-type silicon diodes [3-5] and MOS capacitors in order to assess transient capacitance techniques and other metrological aspects of TSM for characterizing defect levels.

Sulfur was implanted into a diode fabricated by test pattern NBS-2 [3-4] to a dose of 2×10^{14} cm^{-2}. The details of this newly developed technique for introducing pure species into silicon are given in section 3.3.2.3. A part of the wafer was scribed and diced and the gated 1.52-mm (60-mil) diameter base-collector junction (structure 2.9) was mounted with a temperature-sensing diode on a ceramic insulator on a TO-5 header [3-1].

The TSM responses of the sulfur defect centers are shown in figure 3-4. The current responses are for three heating rates, nominally 2, 5, and 10 K/s, and show two current peaks corresponding to two energy levels. The bottom current curve, labeled zero, is the steady-state leakage current curve (obtained by leaving the defect centers uncharged, as described later). The capacitance response curves at the same heating rates and also uncharged are the upper set of curves in the figure. It should be noted that the size of the capacitance step is independent of heating rate and is the same for both levels, but the temperature at which each step occurs shifts with heating rate in the same way that the current peaks shift with heating rate. The size of the current peak increases with increased heating rate.

Analyses of the two sulfur levels were made by the isothermal transient capacitance method procedures which have been developed for the characterization of defect centers. The development is a continuation of the work of Buehler [3-6]. The theory of the method is as follows. The transient decay of the junction capacitance when the bias is changed from zero bias to a reverse bias, V, is controlled in *n*-type silicon by the electron emission rate from defect centers. The net time rate of change of the electron concentration at the defect center is given by [3-7]:

$$\frac{dn_t}{dt} = e_p p_t - e_n n_t \qquad (3\text{-}1)$$

where e_n is the electron emission rate, e_p is the hole emission rate, n_t is the electron concentration at the defect center, and p_t is the hole concentration at the defect center. By use of the totality condition,

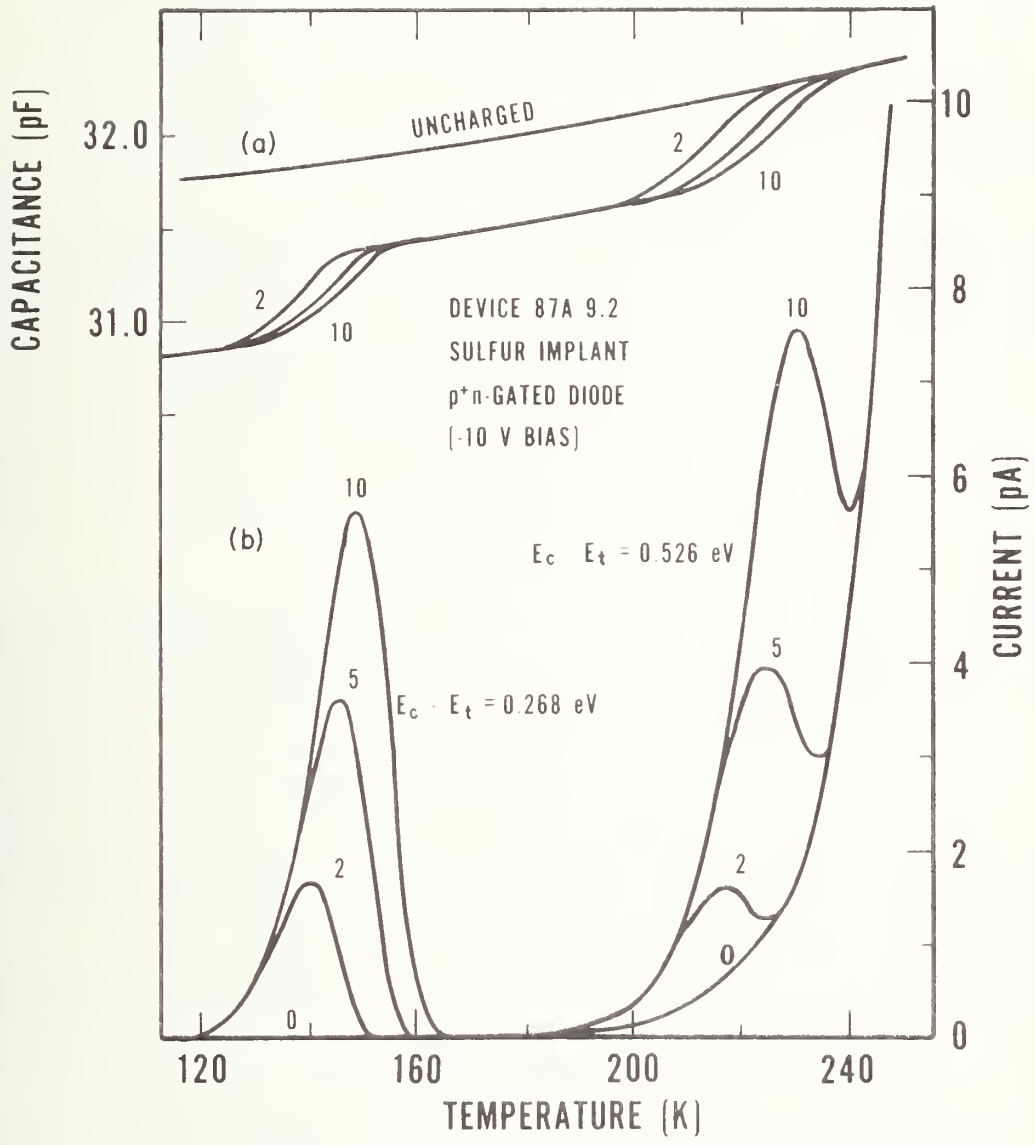

Figure 3-4. Thermally stimulated (a) capacitance and (b) current responses of sulfur defect centers in *n*-type silicon at nominal heating rates of 10, 5, and 2 K/s and zero (steady-state, uncharged condition); E_c is the energy of the conduction band edge and E_t is the energy of the defect.

$$n_t + p_t = N_t \ , \tag{3-2}$$

where N_t is the defect density, a differential equation in n_t can be obtained:

$$\frac{dn_t}{dt} + (e_n + e_p)n_t = e_p N_t \ . \tag{3-3}$$

The general solution is

$$n_t = C_1 \exp[-(e_n + e_p)t] + C_2 \ . \tag{3-4}$$

The constants C_1 and C_2 can be evaluated at times zero and infinity as $C_1 + C_2 = n_t(0) = n_{ti}$ and $C_2 = n_t(\infty) = n_{tf}$. Equation (3-4) can be written

$$n_t = n_{tf} + (n_{ti} - n_{tf})\exp[-(e_n + e_p)t] \tag{3-5}$$

or

$$\frac{n_t - n_{tf}}{n_{ti} - n_{tf}} = \exp[-(e_n + e_p)t] \ . \tag{3-6}$$

Under one-sided step junction conditions, the junction capacitance, C, is

$$C^{-2} = C_b{}^{-2} + \frac{2V}{q\varepsilon A^2(N_d - n_t)} \ , \tag{3-7}$$

where C_b is the junction capacitance at zero bias, A is the junction area, ε is the dielectric constant (permittivity) of silicon, N_d is the dopant density, and q is the electronic charge.

Equation (3-7) can be rearranged as

$$n_t = N_d - \frac{2V\ C_b{}^2C^2}{q\varepsilon A^2(C_b{}^2 - C^2)} \ . \tag{3-8}$$

At t = 0, n_t is n_{ti} and C is C_i. After several time constants, t may be taken as infinite; then, n_t is n_{tf} and C is C_f. Substitution for n_t, n_{ti}, and n_{tf} in eq (3-6) and reduction of the left side to a capacitance ratio, defined as C_r, gives:

$$C_r \equiv \frac{(C_b{}^2 - C_i{}^2)(C_f{}^2 - C^2)}{(C_b{}^2 - C^2)(C_f{}^2 - C_i{}^2)} = \exp[-(e_n + e_p)t] \ . \tag{3-9}$$

The time constant is the value of t when $C_r = \exp[-1]$; $e_n + e_p$ is the reciprocal of the time constant.

The measurement procedure was as follows. At each of seven temperatures in the shallow level range (115.18 to 161.53 K) and nine temperatures in the midgap level range (191.80 to 236.35 K), the device was held at a constant temperature for several minutes at a reverse bias of 5 V and with the peripheral field plate biased into accumulation. The junction bias was then momentarily reduced to zero to collapse the depletion region and charge the defect centers, and then the bias was reapplied during which time a plot of the junction capacitance was recorded against time on one pen of a two-pen X-Y recorder. Pulses from a time-mark generator were applied to the second pen for calibration of the time axis. A typical capacitance transient response is shown in figure 3-5. The time constant of the transient can be estimated from the figure but it can be more precisely determined by the following procedure. The coordinates of 6 to 20 (usually 12) capacitance and time data points were read from the curve and fed into a programmable desk calculator which converted the coordinates into time and capacitance values, calculated the capacitance ratio C_r, plotted the logarithm of C_r against time, made a least squares fit of a straight line to the points, and calculated the time constant. A typical plot is shown in figure 3-6.

For energy levels near midgap, the hole and electron emission rates may be approximately equal in which case additional are required to separate them as described in section 3.3.2.2. For the shallow sulfur level the minority carrier (hole) emission rate is extremely small so that the measured time constant is the reciprocal of the majority carrier (electron) emission rate, e_n. The emission rates can be expressed in the form of the empirical equation of Arrhenius as

$$e_x = B_x T^2 \exp(-\Delta E_x/kT) \quad , \tag{3-10}$$

where x is either n or p, ΔE_n is the energy difference between the defect center and the conduction band, ΔE_p is the energy difference between the defect center and the valence band, k is the Boltzmann constant, and T is the absolute temperature. The prefactor $B_n T^2$ or $B_p T^2$ is equal to the product of the electron or hole thermal velocity, the electron or hole capture cross section, and the density of states in the conduction or valence bands, respectively. When $\Delta E >> kT$, the exponential term dominates the variation with temperature so that the temperature exponent in the prefactor can be assigned any small value. Present experimental precision is not adequate to distinguish between various small values. The choice of the value 2 results from the assumption of a temperature independent cross section.

With e known at several temperatures, an Arrhenius plot of the natural logarithm of e/T^2 against reciprocal temperature, T^{-1}, can be made. The plot has a slope of $-\Delta E_x/k$ and an intercept of $\ell n B_x$. Although e/T^2 is the sum of two pure exponentials, e_n/T^2 and e_p/T^2, over a small tempera-

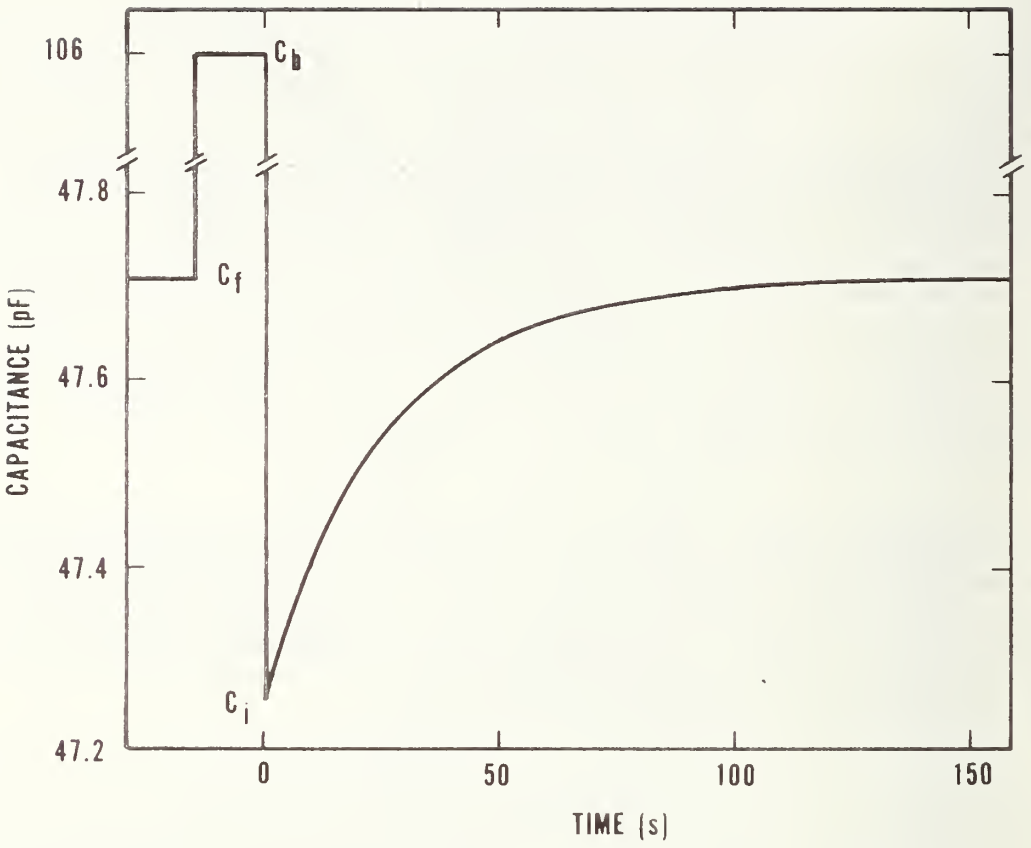

Figure 3-5. Representative isothermal transient capacitance response of a reverse-biased p^+n junction (Device 87AN9.1 at 226.66 K with bias of -5 V).

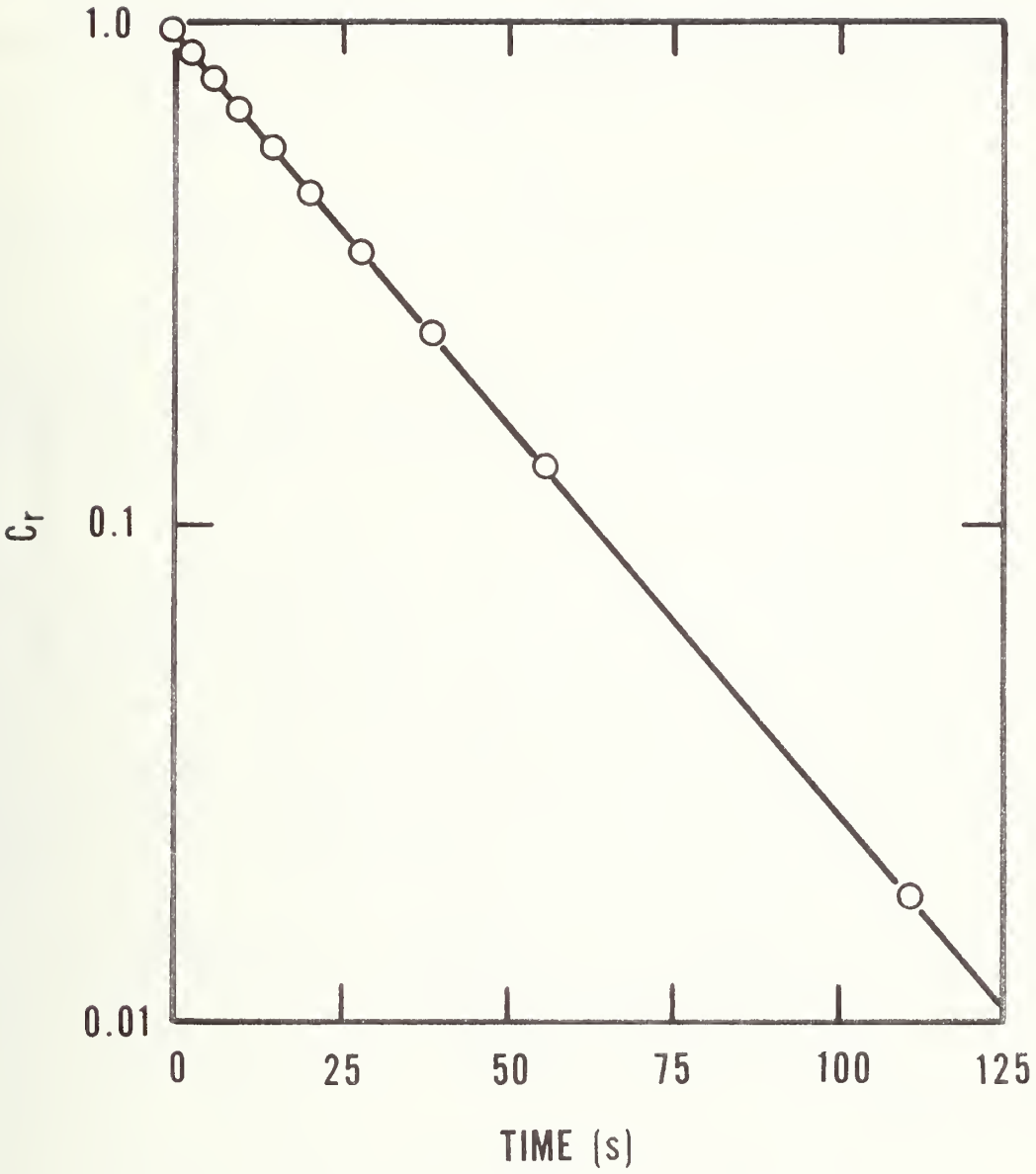

Figure 3-6. Representative semilog plot of capacitance ratio, C_r, against time (same device and conditions as in figure 3-5).

ture range in which one exponential is much larger than the other, the sum also behaves as an exponential.

Plots of the logarithm of e/T^2 against T^{-1} were made for the shallow and the midgap level temperature ranges, and a least squares fit of a straight line to the data points was made with the results for the shallow level shown as circles in figure 3-7:

$$e_n = (9.16 \pm 0.68) \times 10^4\ T^2 \exp[-(0.268 \pm 0.001)/(kT)] , \qquad (3\text{-}11)$$

and for the midgap level (not shown but very nearly the same as the squares in the figure):

$$e = e_n + e_p = (8.81 \pm 0.90) \times 10^6\ T^2 \exp[-(0.526 \pm 0.002)/(kT)] . \qquad (3\text{-}12)$$

These energy levels are in agreement with levels for sulfur introduced by a closed-tube diffusion [3-8], but disagree with one of two levels measured for implanted sulfur after low temperature annealing [3-9].

3.3.2.2 Separation of Electron and Hole Emission Rates

The analysis of the isothermal transient capacitance data for the midgap emission yielded an energy level of 0.526 eV from the sum $e = e_n + e_p$. In that analysis it was implicitly assumed (justifiably) that e_n dominates over e_p and, hence, a reasonable energy level is obtained. However, in cases where the majority and minority carrier emission rates are comparable, it is necessary to separate e_n and e_p in order to ascribe the correct energy to the measured level. Two techniques that in combination with the isothermal transient capacitance method allow this separation are isothermal leakage current measurements [3-7] and isothermal initial and final current [3-10] or capacitance [3-7] measurements.

As an extension of the isothermal capacitance transient measurements, the isothermal initial and final capacitance measurement method was analyzed. Under conditions for which the defect center energy level is several kT from the Fermi level, the defect centers of a reverse-biased junction can be initially fully charged by removing the reverse bias. Then the initial net space-charge density on the *n*-side of a p^+n junction [3-7] is:

$$N_d - N_t = (2V/q\varepsilon A^2)/(C_i^{-2} - C_b^{-2}) , \qquad (3\text{-}13a)$$

and on the *p*-side, where the defect centers are not charged, it is:

$$N_d = (2V/q\varepsilon A^2)/(C_i^{-2} - C_b^{-2}) . \qquad (3\text{-}13b)$$

Again, N_d is the dopant (net acceptor or donor) density, N_t is the defect density, V is the change in bias from the applied bias to the charging (zero) bias, C_i is the initial junction capacitance (with defect cen-

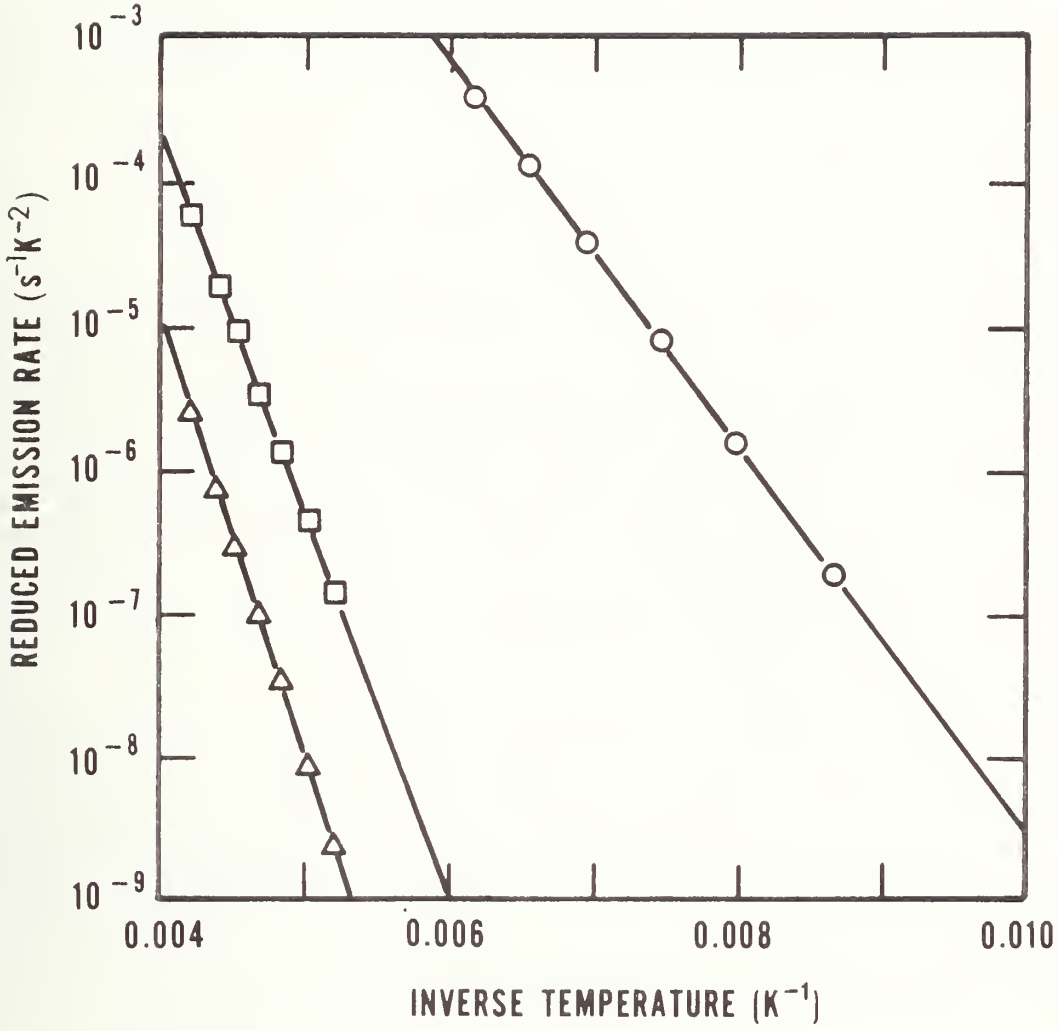

Figure 3-7. Semilog plots of reduced emission rates against inverse temperature for two energy levels of sulfur in *n*-type silicon: ○, e_n/T^2, electron emission from the shallow level; □, e_n/T^2, electron emission from the midgap level; △, e_p/T^2, hole emission from the midgap level (Device 87AN9.2).

ter charged), and C_b is the unbiased junction capacitance. A representative capacitance transient response is shown in figure 3-5.

After discharge, the defect centers return to their steady-state charge density and the net space-charge density on the n-side of a p^+n junction [3-6] is:

$$N_d - N_t e_p/(e_n + e_p) = (2V/q\varepsilon A^2)/(C_f^{-2} - C_b^{-2}) , \qquad (3\text{-}14a)$$

and on the p-side it is:

$$N_d + N_t e_n/(e_n + e_p) = (2V/q\varepsilon A^2)/(C_f^{-2} - C_b^{-2}) , \qquad (3\text{-}14b)$$

where C_f is the final (steady-state) junction capacitance. Subtraction of eq (3-13a) from eq (3-14a) or eq (3-13b) from eq (3-14b) gives the same result [3-6]:

$$\frac{N_t e_n}{e_n + e_p} = \frac{2V}{q\varepsilon A^2} \frac{C_b^4 (C_f^2 - C_i^2)}{(C_b^2 - C_f^2)(C_b^2 - C_i^2)} . \qquad (3\text{-}15)$$

This can be arranged to give the ratio of hole to electron emission rates in the p^+n junction:

$$\frac{e_p}{e_n} = \frac{N_t q\varepsilon A^2}{2V} \cdot \frac{(C_b^2 - C_f^2)(C_b^2 - C_i^2)}{C_b^4 (C_f^2 - C_i^2)} - 1 . \qquad (3\text{-}16)$$

Hence, e_n and e_p are separable by use of eqs (3-9) and (3-16).

An independent, accurate measurement of N_t is required to evaluate e_p/e_n. A dynathermal thermally stimulated capacitance measurement will give the N_d/N_t ratio (see Appendix B of [3-1]), and N_d is known from the resistivity of the material (or it can be measured; see section 3.3.3.2). It can be seen from eq (3-16) that the uncertainty in the ratio e_r/e_n is greater than the fractional uncertainty of the N_t determination. Therefore, very small values of e_r/e_n are not reliably measurable.

Isothermal capacitance-leakage current measurements can be used to check the analysis described above. The isothermal reverse leakage current and the corresponding capacitance are measured over a range of reverse bias voltages at each of several temperatures. At each temperature, the slope is obtained of a straight line fitted by least squares to the leakage current plotted against reciprocal capacitance for various biases. The slope divided by qA is the generation rate G, which is a function of temperature [3-11]:

$$G(T) = N_t e_n e_p/(e_n + e_p) . \qquad (3\text{-}17)$$

Substitution of $N_t e_n/(e_n + e_p)$ from eq (3-15) into eq (3-17) gives e_p which can be subtracted from e in eq (3-12) to obtain e_n at each temperature. Arrhenius plots again give the parameters ΔE_x and B_x.

The above procedures were tested experimentally by separating the midgap electron and hole emission rates of the same sulfur-implanted *n*-type silicon diodes which were used for the isothermal transient capacitance measurements. At each temperature, the following quantity, a rearrangement of eq (3-15), was calculated:

$$\frac{N_t}{1 + \frac{e_p}{e_n}} = \frac{2V}{q\epsilon A^2} \frac{C_b^4 (C_f^2 - C_i^2)}{(C_b^2 - C_f^2)(C_b^2 - C_i^2)} . \qquad (3\text{-}18)$$

For a circular junction of diameter 1.52 mm (60 mil), with V = 5 V and $N_t = 1.55 \times 10^{13}$ cm^{-3} (measured on the shallow level where $e_p \approx 0$), the ratio e_p/e_n was calculated from the experimental values of the capacitances. Because the ratio is extremely sensitive to the difference $C_f - C_i$ and sensitive to the individual values of C_i and C_f, it was necessary to smooth the experimental values by making a least squares fit of the data against temperature. The smoothed values of C_i and C_f were typically within 0.01 pF of the experimental values and the Pearson's linear correlation coefficients of the fits were 0.999 for each. The fit of C_b was not as good, 0.998, but the ratio was not sensitive to smoothing C_b.

The electron emission rate, e_n, was calculated by dividing the isothermal transient capacitance values for $e_n + e_p$ by $(1 + e_p/e_n)$. The calculated value of e_n was multiplied by the e_p/e_n ratio to obtain e_p.

Plots of the logarithm of e_n/T^2 and e_p/T^2 were made and analyzed. The midgap electron emission rate (shown as squares in fig. 3-7) can be characterized by:

$$e_n = (7.54 \pm 0.76) \times 10^6 \, T^2 \exp[-(0.524 \pm 0.002)/(kT)] \qquad (3\text{-}19)$$

and the hole emission (shown as triangles) by:

$$e_p = (1.76 \pm 0.35) \times 10^7 \, T^2 \exp[-(0.604 \pm 0.003)/(kT)] . \qquad (3\text{-}20)$$

The sum of the electron activation energy of 0.524 eV to the conduction band and the hole activation energy of 0.604 to the valence band is 1.128 eV and is close in value to the silicon band gap. This agreement supports the validity of the energy characterization. The difference in energy determined from $e = e_n + e_p$ (0.526 eV) and the separated value of e_n (0.524 eV) is statistically insignificant for this case of the midgap sulfur level. However, this example clearly demonstrates the separation technique, and the method would be important for cases where e_n and e_p for a given level are approximately equal.

3.3.2.3 *Ion Implantation as a Means for Introducing Defect Centers in Silicon**

Another important aspect in the development of measurement methods is the necessity to fabricate appropriate devices in which the measurements could be made. A technique which is common to power device processing for lifetime control is the diffusion of gold or platinum from a spin-on or plated (evaporated) coating. Another technique used for controlled introduction of impurities in integrated circuits fabrication is ion implantation. The ion implantation technique offers significant advantages over the standard diffusion technique: 1) controlled purity of the implant species, 2) controlled dose, and 3) wide selection of implantable impurities. Because of these advantages, the capabilities for using ion implantation to fabricate samples for deep level studies was developed.

The sulfur samples described in sections 3.3.2.1 and 3.3.2.2 and also discussed in section 3.3.3.2 were prepared by ion implantation. The test structures were fabricated on nominal 5 to 10 Ω·cm, <111>, n-type silicon wafers using test pattern NBS-2 [3-4]. Boron predeposition was made through 60-mil (1.52-mm) and 81-mil (2.06-mm) openings in 500 nm of field oxide; a subsequent drive-in was used to form a 450-nm deep p^+ region and to regrow approximately 30 nm of oxide over the p^+ region to seal the wafer. Sulfur ions were implanted at an energy of 140 keV (or 280 keV for S_2^+) by rastering the ion beam over the wafer surface. By selection of the energy, ion penetration into the silicon was allowed only in the regions of the thin-oxide openings over the p^+ diffusions. The estimated peak of the sulfur distribution was 120 nm below the silicon surface with a projected standard deviation of approximately 57 nm [3-12]. This sulfur predeposition implant within the p^+ deposition was followed by a 10-min, 1000°C anneal in dry nitrogen to remove the primary implant damage and to diffuse the sulfur toward the junction. Approximately 150 nm of silicon dioxide was chemically vapor deposited at 400°C to increase the thickness of the oxide over the diffusions. This was followed by a 10-min, 1000°C heat treatment in dry nitrogen to densify the deposited oxide and further diffuse the sulfur. Contact cut, front-surface metallization (aluminum), back-surface metallization (gold plus 0.6-percent antimony), front-surface metal definition, and a 10-min, 500°C microalloy in dry nitrogen completed the fabrication of the structures. The near surface pn junction boundary is located under the thick field oxide due to lateral diffusion during junction formation so that the boundary is protected from implantation damage. A field plate around the diode was provided to control any leakage around the junction periphery.

The use of ion implantation for deep level studies has a number of significant facets which should be reemphasized. In particular, ion implantation in this study was used as a controlled predeposition step; that is, a known amount of impurity was implanted into the diffused re-

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* Funded by the Defense Advance Research Projects Agency through ARPA Order No. 2397, Program Code 7D10, and by NBS.

gion to a very shallow depth. Because the implantation was shallow, implantation damage was confined to a region far from the actual junction boundary. In addition, because of the lateral diffusion of the boron during junction formation, little or no implantation damage occurred near the intersection of the junction with the surface. Finally, a standard thermal heat treatment was used to diffuse the implanted ions to the junction regions and into the bulk, as well as to anneal the implantation damage which occurred in the implant region. The results on the sulfur-implanted wafers which were described earlier demonstrated the use of this ion-implant predeposition and diffusion technique for fabrication of deep level samples. It opens the door for a great variety of defects which could be studied by the deep level techniques.

3.3.3 Extension of Thermally Stimulated Measurement Techniques to Deep Level Transient and Defect Profiling Measurements

3.3.3.1 Transient Capacitance Technique

The detection of deep level defects in semiconductors by the measurement of depletion capacitance transients has been utilized by a number of people using several experimental methods (e.g., see [3-1],[3-2],[3-6], [3-7],[3-13],[3-14]). In the traditional thermally stimulated capacitance (TSCAP) measurement [3-7],[3-13] defects charged at low temperatures are induced to discharge by heating the device. In the deep level transient spectroscopy (DLTS) technique [3-2], the device is continually pulsed to charge the defect, and the discharge is continually detected as the device temperature is changed slowly. A third technique, the isothermal transient capacitance (ITCAP) technique (see previous discussion and [3-6]), directly detects the discharge transient after the device is switched from charging bias to depletion bias with fixed temperature. Whereas DLTS utilizes an rf bridge (20 MHz) [3-14] for its capacitance measurement, both TSCAP and ITCAP are typically performed with a commercial 1-MHz capacitance bridge. All three methods are capable of determining the density, energy level, and emission rate ($e = e_n + e_p$) for the defect.

The ITCAP method was extended to combine the use of a commercial 1-MHz capacitance bridge with the continually pulsed bias technique from DLTS. A digital processing oscilloscope, in conjunction with a minicomputer, is used to capture the capacitance transient and perform computations to characterize the transient. This extension allows more rapid data analysis and the measurement of shorter emission decay rates than are achieved with the conventional ITCAP method. In addition, it constitutes a rapid technique for measuring defect densities for wafer mapping purposes.

Figure 3-8 shows a typical series of bias pulses and the resulting capacitance transients. A p^+n junction structure is assumed for specificity and only majority carrier charging [3-2] is assumed for simplicity. The large capacitance pulse accompanying the zero-bias voltage pulse is due to the momentary collapse of the depletion region which allows charging of the traps. After depletion is reestablished, the charged traps will emit carriers at a rate governed by the temperature; the initial capaci-

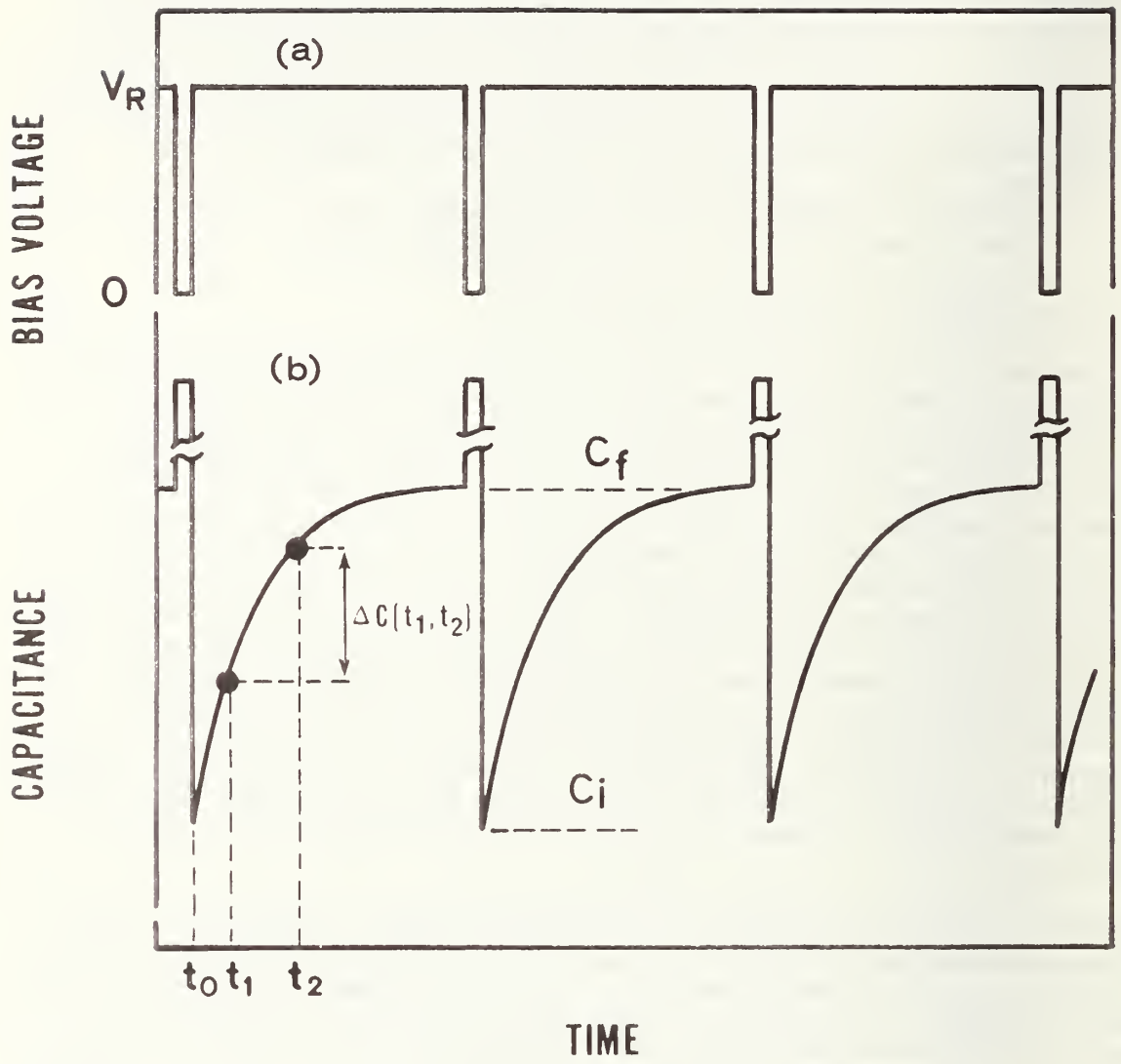

Figure 3-8. Schematic representation of (a) the pulsed applied voltage and (b) the resulting capacitance transient.

tance C_i will decay to a final value C_f. This behavior can be modeled as:

$$C(t,T) = C_f - (C_i - C_f)e^{-et} , \qquad (3\text{-}21)$$

where C is the time and temperature dependent capacitance, T is the absolute temperature, t is the time, and e is the emission rate. In the DLTS mode of operation, the change in capacitance $\Delta C(t_1,t_2)$ (see fig. 3-8) is monitored as a function of the temperature. This is typically done with a dual-channel box car integrator with the gate time set at known times t_1 and t_2. An inherent advantage of DLTS is its use of the high frequency bridge to increase the measured signal. In the usual ITCAP measurement, a single capacitance transient is captured on a recording medium such as an X-Y recorder. Response time of the recorder and signal-to-noise ratio generally limit this measurement to decay times in excess of 100 ms.

A schematic diagram of the modified ITCAP experiment is shown in figure 3-9. In this mode of operation, the device-under-test is maintained at a fixed temperature and continually pulsed as indicated in figure 3-8. The dc depletion bias is applied to the device via the "LO BIAS" input of a commercial 1-MHz capacitance bridge. The charging pulses are applied in series with the device via a pulse transformer on the "LO" side of the input. In order to utilize fully the useful dynamic range of the digital processing oscilloscope, it is necessary and desirable to suppress the large, zero-bias capacitance signal of interest. This is simply accomplished by gating the output of the capacitance bridge with an analog gate (integrated circuit type 4016); the gate signal time and duration are adjusted by tuning the output widths of the GATE DELAY (IC type 74121) and the GATE WIDTH (IC type 74121) controls.

Figure 3-10 shows three typical signals observed during operation of the circuit. The device under test was a p^+n gold-diffused diode. The gate signal applied to the analog gate is shown in figure 3-10a and appears at the point marked (1) in figure 3-9. The adjustable GATE DELAY is convenient for optimum setting of the gate position with pulse generators which have an adjustable pulse delay between "sync out" and "pulse out." The device-under-test was held at a 15-V reverse bias and pulsed to zero bias with a 1-μs wide pulse. The ungated analog signal from the capacitance bridge is shown in figure 3-10b and appears at (2) in figure 3-9. It features the large zero-bias capacitance pulse during the charging; the width of this capacitance pulse is indicative of the response time of the capacitance bridge (<1 ms). The gated capacitance transient is shown in figure 3-10c and appears at point (3) in figure 3-9. An adjustable capacitor applied to the "differential" terminal of the capacitance bridge is adjusted to null the steady-state reverse bias capacitance (i.e., C_f). This allows the bridge to be used on a higher sensitivity range to provide higher amplification for the oscilloscope in a direct-coupled mode. The signal-to-noise ratio for the three traces in figure 3-10 was enhanced by averaging the signal over 100 transients by use of

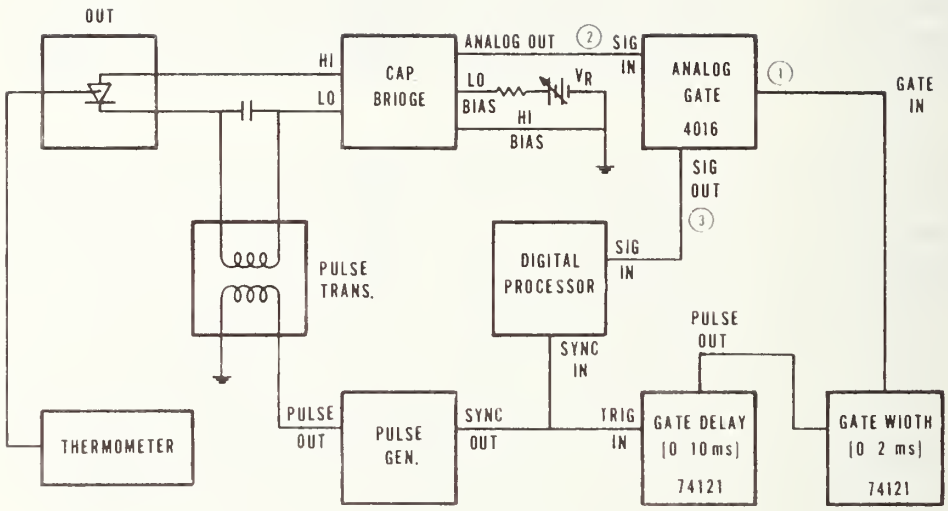

Figure 3-9. Circuit diagram for the pulsed isothermal transient capacitance measurement.

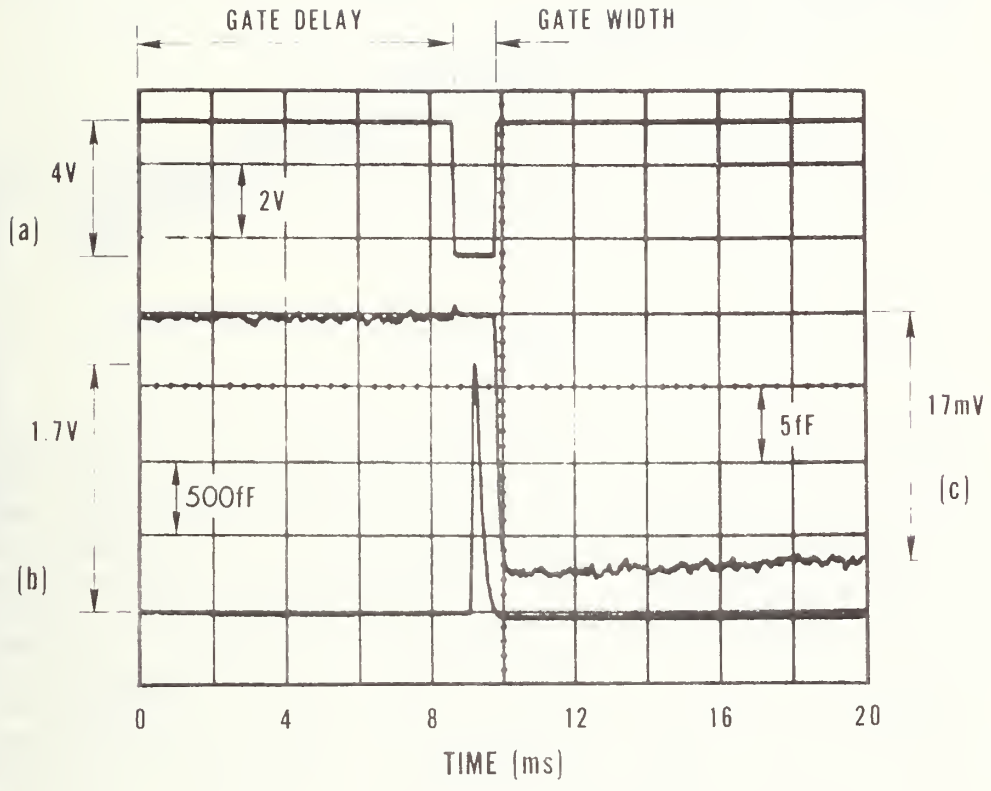

Figure 3-10. Oscilloscope traces of (a) the gate pulse, (b) the ungated capacitance transient, and (c) the gated capacitance transient (each trace is the average of 100 scans). The device-under-test was a $p^{+}n$ gold-diffused diode.

the capabilities of the digital processing oscilloscope and the minicomputer.

Figure 3-11a shows the same gated capacitance transient on an extended time scale. It represents a single sweep of the oscilloscope and shows the inherent noise of the system. In figure 3-11b, the same signal appears after averaging over some 2000 transients. The improvement in signal-to-noise ratio is obvious. The analysis to calculate the emission rate e given in eq (3-21) was based on the averaged capacitance transient. Note that in calculating the time constant (e^{-1}) of the exponential decay of figure 3-11b, the actual values of C_f and C_i are unimportant. Hence, for simplicity, the transient can really be modeled as:

$$y = -y_o \, \varepsilon^{-et} \quad . \tag{3-22}$$

This is equivalent to displacing the curve vertically so that $C_f = 0$ and $C_i = y_o$. Then the following manipulations can be performed to calculate e:

$$\frac{1}{y} \cdot \frac{dy}{dt} = \frac{y_o e \, \varepsilon^{-et}}{-y_o \, \varepsilon^{-et}} = - e \quad . \tag{3-23}$$

Figure 3-12 shows the emission rate as calculated by the algorithm represented in eq (3-23). The increase in noise as a function of time is due to the statistical increase in the uncertainty of the signal as the transient gets smaller with time. The absence of the differential discontinuity at the beginning of the transient and the abrupt zero near the end of the transient are due to software manipulations to avoid overdriving the dynamic range of the processor. The relative "flatness" of the calculated emission rate shown in figure 3-12 is indicative of the true exponential behavior of the curve. Note that in adjusting the repetition period of the applied pulses, it is necessary to insure that equilibrium to C_f has, in fact, been established. Otherwise, the algorithm used to calculate the emission rate would be incorrect. A number for the emission rate is obtained by simply taking an average over the relevant range of figure 3-12. In this case, the emission rate is calculated to be 3.3 s^{-1} at a temperature of 238 K and is in good agreement with the data of Sah *et al.* [3-10] for electron emission from the gold acceptor (for the gold acceptor, the electron emission rate is about an order of magnitude higher than the hole emission rate [3-10]).

The method described here offers a straightforward technique for measuring emission rates from defect centers as a function of temperature. This in turn can allow one to calculate the effective energy level for such defects. This procedure is equivalent to the isothermal transient capacitance method discussed in section 3.3.2.1, and therefore is not as precise as the method discussed in section 3.3.2.2.

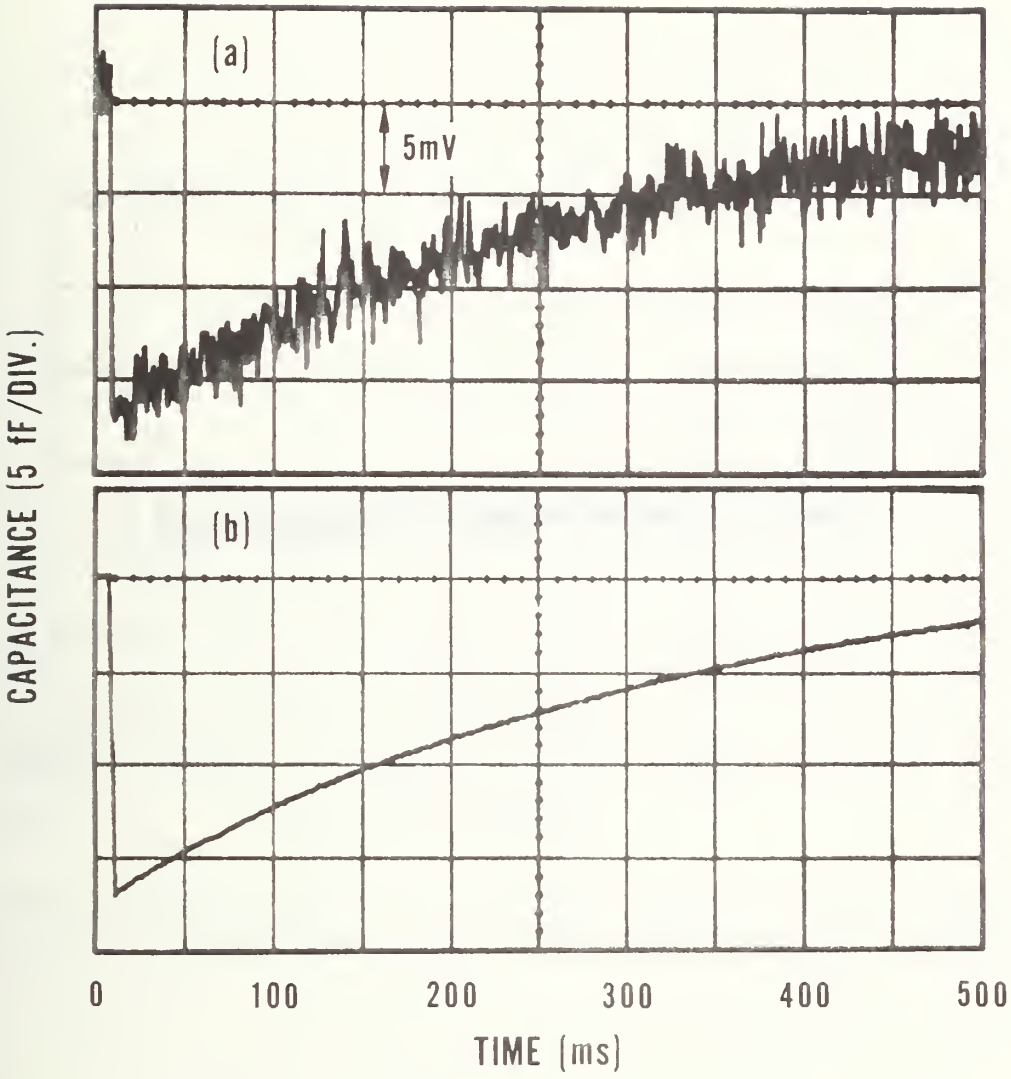

Figure 3-11. Oscilloscope traces of (a) a single-gated capacitance transient and (b) the gated capacitance transient averaged 2000 times.

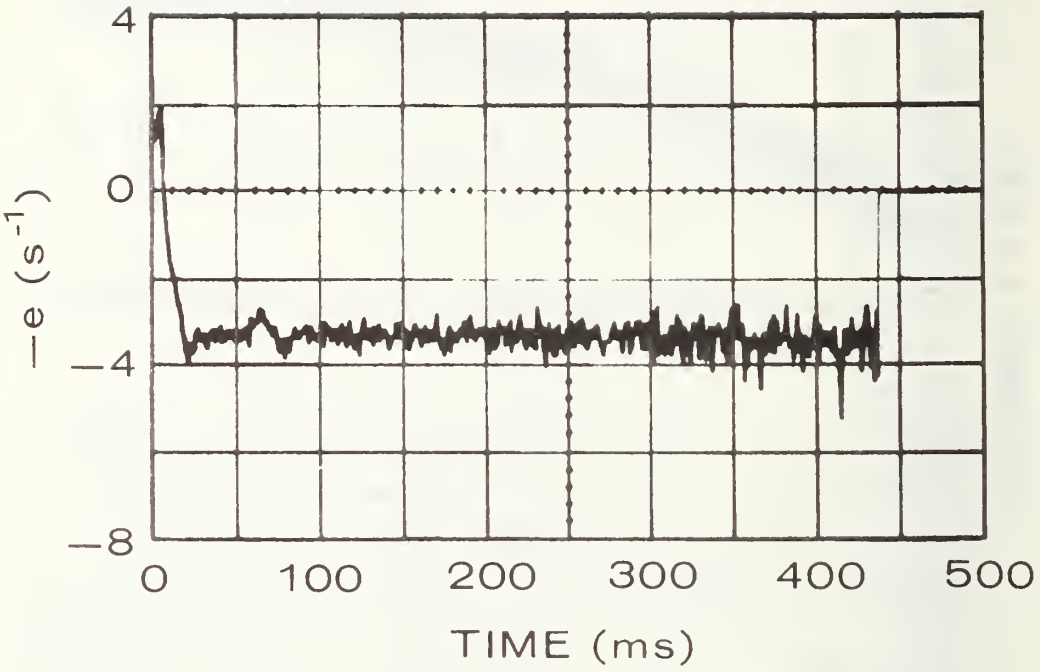

Figure 3-12. Oscilloscope trace of the calculated emission rate determined from eq (3-23). The average value is $e = 3.3\ s^{-1}$.

In addition, the technique also offers an alternative way to determine the defect density without the necessity to cycle the sample temperature as is done in the usual thermally stimulated capacitance measurement. This is done by specifically retaining the absolute values of C_f and C_i and calculating the defect density as described previously [3-3, p. 44]. Hence, it would be possible to perform defect wafer map measurements in a considerably shorter time period.

3.3.3.2 Defect Profiling Technique

Lifetime of minority carriers in power devices is an important parameter which controls the forward voltage drop and the switching characteristic of devices. For purposes of modeling the forward drop, a prime consideration is the lifetime or defect profile through the entire thickness of the thyristor. A knowledge of the intentional defect density profile provides information which is basic to the lifetime profile.

A procedure was developed and tested for measuring defect depth profiles in a semiconductor junction in order to evaluate the feasibility of using TSM for defect profiling. In brief, the procedure consists of establishing a depletion region by reverse biasing the junction at room temperature, turning off the defect center emissions by cooling the junction to a low temperature, incrementally collapsing the depletion region by decreasing the bias in steps to zero, and then incrementally reestablishing the depletion region by increasing the bias in steps. The net dopant density can be calculated at each incremental level from the variation of capacitance with bias, first in collapsing the depletion region with the defect centers nearly empty, and then in restoring the depletion region with the defect centers charged. The difference in the net dopant density under charged and uncharged conditions gives the defect density, and the dopant density can be obtained from the variation of capacitance with bias in the uncharged condition. The distance coordinate is obtained from an average value of capacitance appropriate to the incremental level. The procedure is suitable for either automated or manual measurements. Details of the procedure follow.

A junction is reverse biased at room temperature and then cooled under that constant bias to a temperature well below the emission temperature of the defect center being evaluated. Then with the temperature maintained constant, the bias is monotonically decreased in convenient steps (with a minimum step of perhaps half a volt) to zero bias and, at each voltage step, the junction capacitance and bias voltage are carefully measured to at least four (preferably to five) significant figures to minimize roundoff errors. The bias is then increased in steps to the beginning value and the measurements are repeated at each step. The monotonically decreasing voltages are designated V_n, for n = 0 to N, where $V_N = 0$, and the corresponding capacitances are designated C_n; the increasing voltages (not required to be monotonic because the defect centers are now charged and will remain charged) are designated V_m, with corresponding capacitance C_m. There are two alternative ways to simplify the procedure: 1) use the same voltage steps, $V_m = V_n$, or 2) use the

same capacitance values, $C_m = C_n$. For each value of V_n and V_m, the quantities C_n^{-2} and C_m^{-2} are calculated. The local slope of a plot of C^{-2} against V (shown in figure 3-13 for $V_m = V_n$ and for an idealized case of uniform dopant and defect densities) is calculated for each increment; namely, $(C_{n-1}^{-2} - C_n^{-2}) \cdot [|V_n - V_{n-1}|]^{-1}$. The net dopant density is inversely proportional to the slope. The net dopant density for decreasing bias is $N_d - n_{tf}$ and for increasing bias is $N_d - n_{ti}$, and the proportionality constant is $(2/q\epsilon A^2)$. Again, n_t is the electron density at the defect center, subscripts f and i denote final (uncharged) and initial (charged) conditions of thermal emission, and the nomenclature assumes an n-type semiconductor depletion region. The equations are:

$$N_d - n_{tf} = \frac{2}{q\epsilon A^2} \frac{|V_n - V_{n-1}|}{C_{n-1}^{-2} - C_n^{-2}} \tag{3-24}$$

and

$$N_d - n_{ti} = \frac{2}{q\epsilon A^2} \frac{|V_m - V_{m-1}|}{C_{m-1}^{-2} - C_m^{-2}} . \tag{3-25}$$

Under the experimental conditions described, n_{ti} is N_t, the defect density, and n_{tf} is the steady-state equilibrium defect density, $N_t e_p/(e_n + e_p)$. Subtraction of eq (3-25) from eq (3-24) gives:

$$N_t \frac{e_n}{e_n + e_p} = \frac{2}{q\epsilon A^2} \left[\frac{|V_n - V_{n-1}|}{C_{n-1}^{-2} - C_n^{-2}} - \frac{|V_m - V_{m-1}|}{C_{m-1}^{-2} - C_m^{-2}}\right] . \tag{3-26}$$

Except for midgap levels, the minority carrier emission rate (e_p for n-type as assumed here) can be assumed negligible compared with the majority carrier emission rate (e_n) in which case N_t is given directly by eq (3-26). In general, if the carrier emission rates are known for the defect, the ratio $e_n/(e_n + e_p)$ can be calculated. Although the appropriate temperature at which to calculate the ratio is a slight function of the cool-down rate (see fig. 1 of [3-1]), the emission temperature for the heating rate used is satisfactory. If the carrier emission rates are not known, they may be found from the procedure illustrated in the section 3.3.2.2.

Equation (3-25), with $n_{ti} = N_t$ can next be used to calculate N_d at each voltage increment. The corresponding depletion depth, W, can be calculated from the average capacitance in each increment. Although the best way to calculate the average has not been determined, the average values of C^{-2} can be used as a first approximation to calculate W. This gives:

$$W = 0.5\epsilon A \left(C_{n-1}^{-2} + C_n^{-2} - C_{m-1}^{-2} + C_m^{-2}\right)^{0.5} . \tag{3-27}$$

A plot of the values of N_t and N_d as a function of W gives the one-dimensional (depth) defect and dopant profiles.

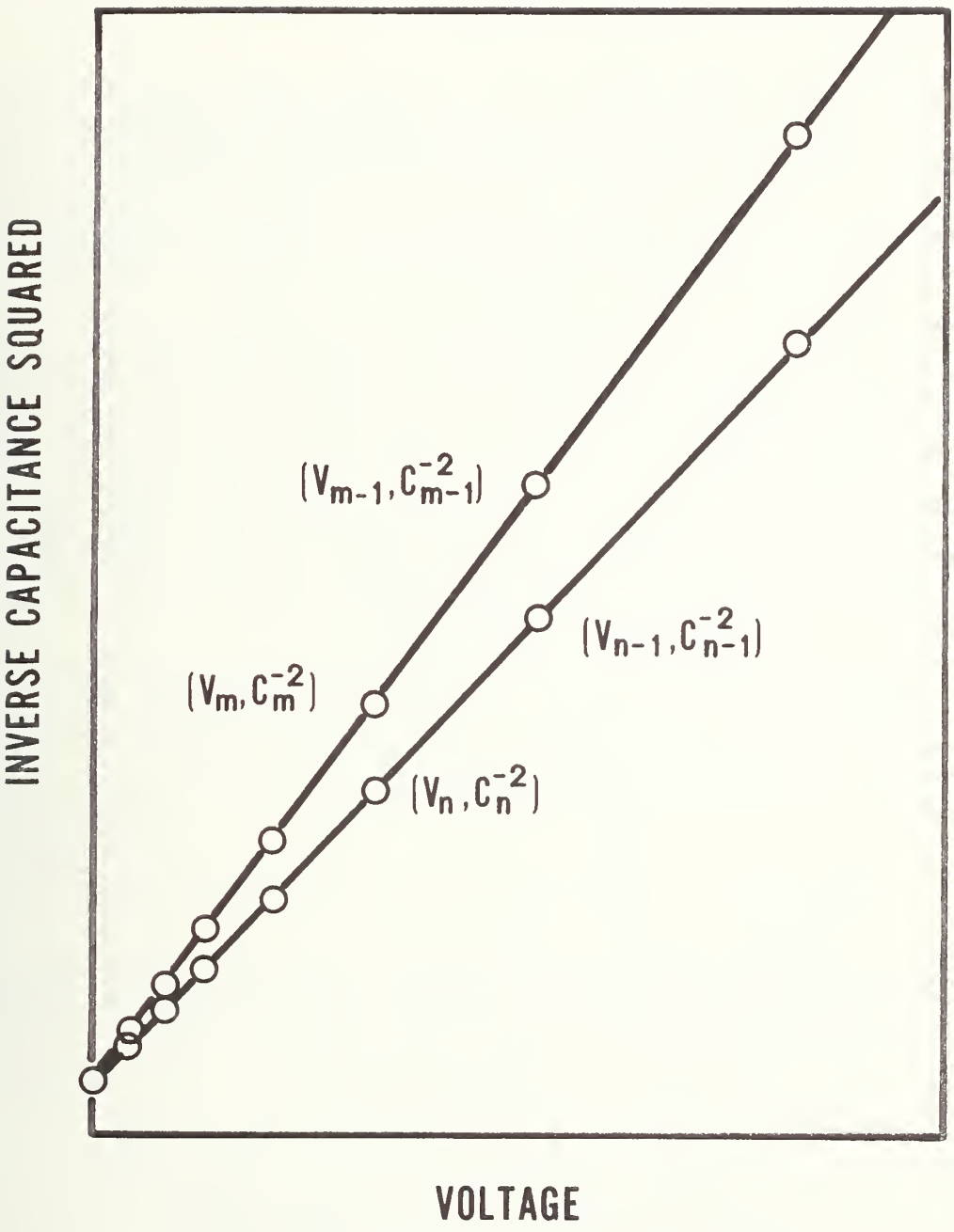

Figure 3-13. Schematic C^{-2} versus V curves with defect centers uncharged (bottom line) and charged (top line).

The defect profiling procedure was tested on a sulfur-implanted p^+n junction, structure 2.19 of test pattern NBS-2 [3-4]. Sulfur was implanted in the 81-mil (2.06-mm) diameter diode to a dose of 1×10^{13} cm^{-2} and the diode was mounted on a TO-5 header. The details of the fabrication procedure are given in section 3.3.2.3.

The diode was reverse biased by 20 V at room temperature and cooled to liquid nitrogen temperature. The peripheral field plate bias was adjusted to minimize the reverse leakage current. The junction bias was reduced in approximately 2-V increments to zero bias and at each voltage step the capacitance and bias were measured to five significant figures. The bias was then increased by steps so as to duplicate the decreasing capacitance values and the required bias was measured at each step.

These data were fed into a programmable desk calculator which calculated eqs (3-24) through (3-27) with $C_m = C_n$, plotted C_n^{-2} against V_n and C_m^{-2} against V_m (straight lines as in fig. 3-14 except that the slopes are nearly equal; not shown), and made a semilog plot of N_t and N_d against the depletion depth W (fig. 3-14). The dopant density is very uniform with a value of $(9.54 \pm 0.12) \times 10^{14}$ cm^{-3}. The defect density profile shows a larger scatter because it is obtained from the difference of eqs (3-24) and (3-25) whose values are about 200 times larger than their difference. Despite the statistical scatter, it is apparent that the defect density is essentially uniform with a value of 5×10^{12} cm^{-3}.

These results suggest that defect profiling by this technique is feasible. However, it is necessary to be extremely accurate in making the measurements. The present results were obtained by manual methods. Automation procedures and further studies will be necessary to simplify the method, to improve the statistical precision and accuracy, and to increase the speed of the measurement.

3.3.4 Correlation of Defect Density with Electrical Parameters (Objective 3.3)

To date, the objective of these deep level studies has been to detect and characterize defects in the depletion region of silicon structures. The next step is to relate the presence of specific defects to measurable electrical operating parameters of the device. This correlation of the active defect density to the device performance is an important link in the measurement and control of active defects.

An important performance specification for all rectifier diodes and thyristors is the off-state current or the reverse leakage current, I_R. Under reverse bias conditions, the total current through the junction is the sum of space charge generation current and diffusion current generated in the neutral region within a diffusion length of the depletion edge. The diffusion current is negligible [3-15] at the temperature used in these deep level studies. A simplified expression for the space charge generation current is given by [3-15]:

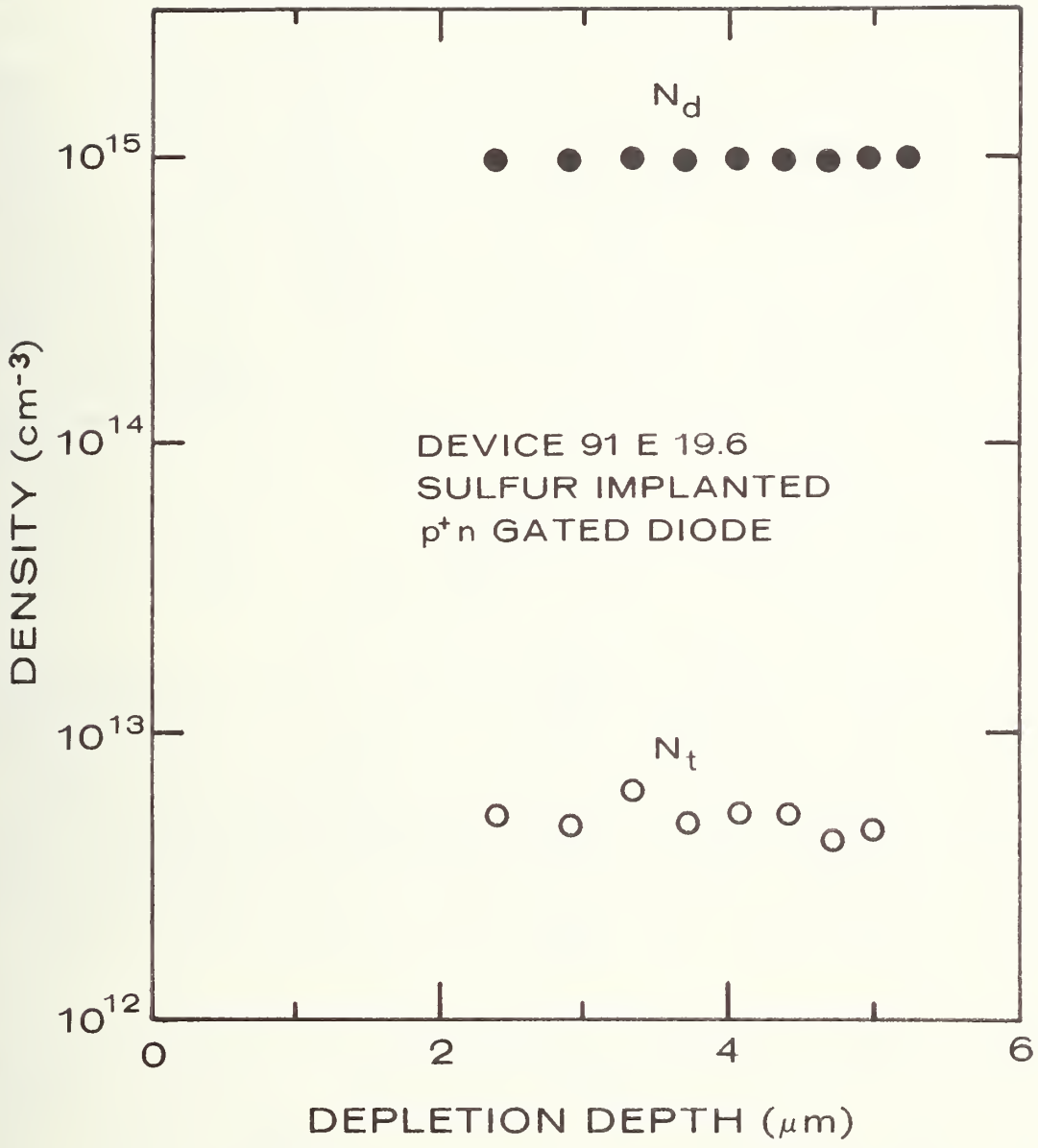

Figure 3-14. Defect density N_t and dopant density N_d profiles.

$$I_{gen} = \frac{q\ K\ N_t\ W\ A}{2\ \cosh\ [(E_i - E_t)/kT]}\ , \qquad (3\text{-}28)$$

where N_t is the trap (recombination-generation center) density, E_i is the intrinsic Fermi energy, E_t is the trap energy, W is the space charge width, and K is the product of the intrinsic carrier concentration, the thermal carrier velocity, and the capture cross section (simplified by assuming that electron and hole capture cross sections are equal).
For this study, the thermally stimulated current and capacitance measurement (TSM) technique was used to determine the defect density of a gold-doped wafer processed with p^+n gated diodes. After the planar diodes were fabricated on an n-type wafer, the gold was deposited on the back surface and diffused for 24 h at 800°C. Figure 3-15 shows a current and capacitance response of a typical device on the wafer. The defect response causing the capacitance transition and current peak near 225 K is due to emission from the gold acceptor near midgap at 0.547 eV below the conduction band edge. After the acceptor emission, the device is clearly seen to enter the temperature-dependent reverse-leakage regime. This is also clear evidence that leakage in the gold-doped diode occurs through the midgap acceptor level. The thermally stimulated capacitance technique [3-3, pp. 42-44] was used to map the density of the gold acceptor defect as a function of position on the wafer (see fig. 3-16a). The wafer map graphically reveals the nonuniformity of the distribution of the active gold defects. The defect density varies from 1.89 to 7.55 × 10^{13} cm^{-3}, increasing from light to dark regions. (There are five symbols representing equal intervals between 1.89 and 7.55.)

The room temperature reverse leakage current for the same devices was also measured. The temperature was maintained at 23°C and the applied bias was -15 V. The results illustrated in figure 3-16b show a variation in the leakage from 0.257 to 1.045 nA. The patterning of the current leakage wafer map is virtually identical to the gold acceptor defect density. Where the defect density is low, the leakage current is low. Plotted in figure 3-17 is the reverse leakage current against the acceptor defect density. Each point represents one of the 65 devices on the wafer. Although there is scatter, there is an obvious near-linear relationship between the reverse leakage current and the defect density.

In an earlier study of the gold donor in p-type silicon [3-3, p. 45], a map of the gold donor defect in a particular wafer showed only a 50-percent variation from 2.34 to 3.61 × 10^{13} cm^{-3}. A reverse leakage measurement was also made on this wafer and plotted. The data points all fall within the rectangle shown in figure 3-17. Again, there was scatter of these data; however, it is clear that the leakage current of these n^+p devices essentially falls on the same plot and shares the same relationship as the p^+n devices. The gold donor is a shallow level (0.345 eV above the valence band), and hence its emission occurs at temperatures well below the onset of reverse leakage (see [3-3, p. 43]). Therefore, the donor defect cannot influence the reverse leakage. However, since the data for the gold donor in the n^+p devices fall essentially on

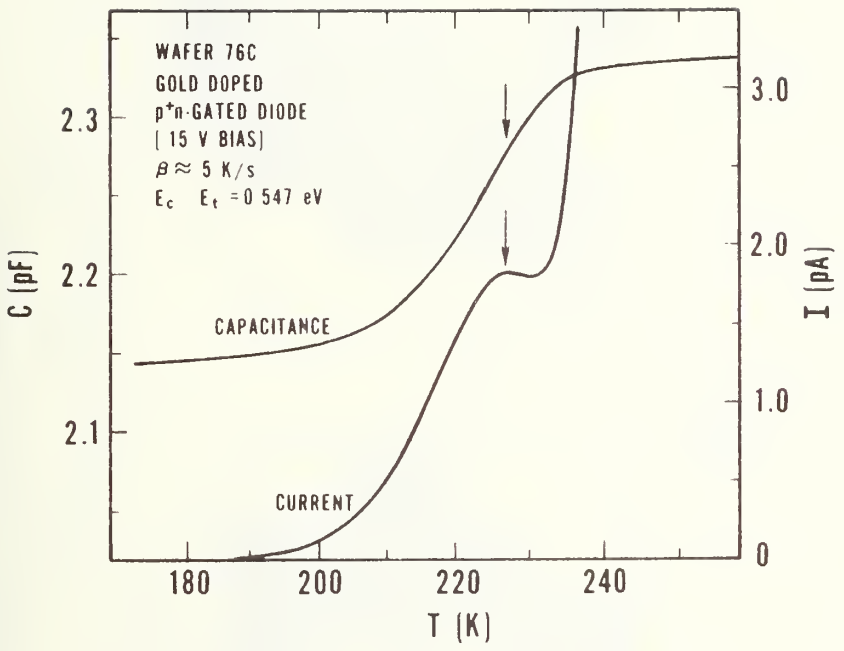

Figure 3-15. Thermally stimulated capacitance and current response of the midgap gold acceptor. The heating rate is about 5 K/s.

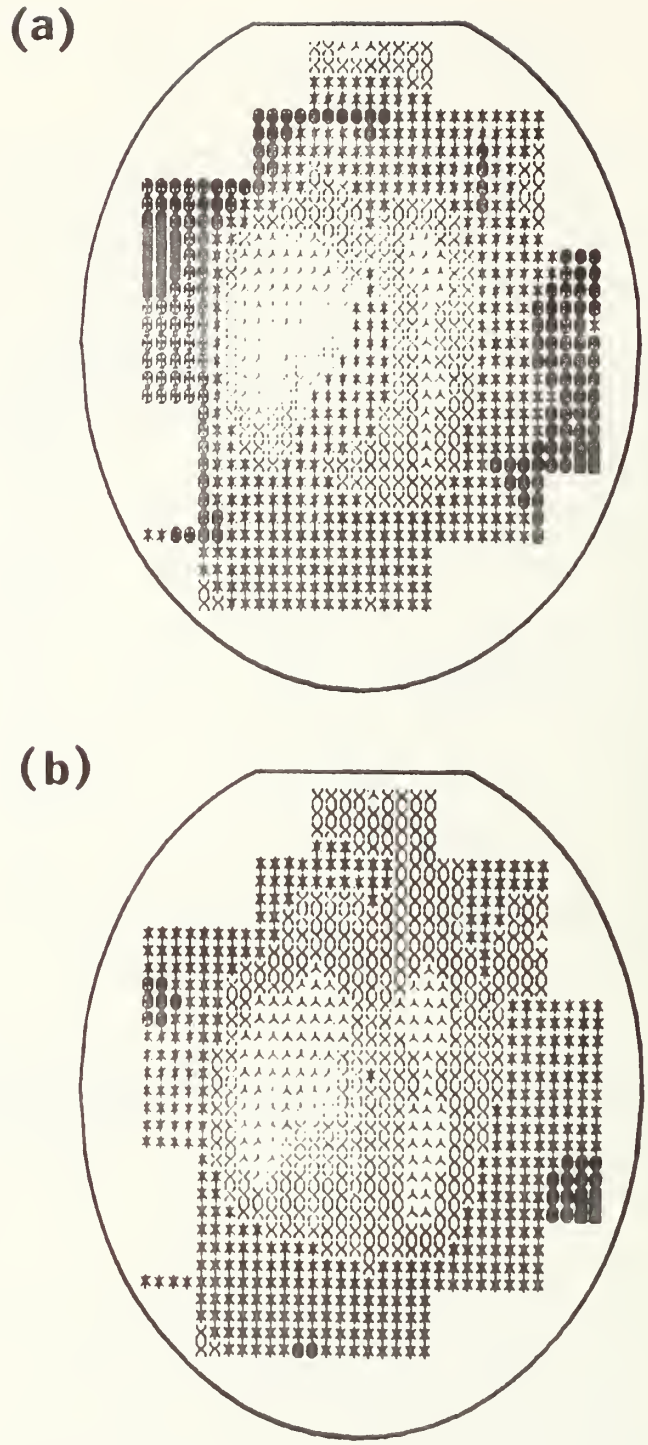

Figure 3-16. Wafer maps of (a) the gold acceptor defect density and (b) the reverse leakage current. Approximately 65 devices spaced at 5.08-mm intervals on the 51-mm wafer were measured.

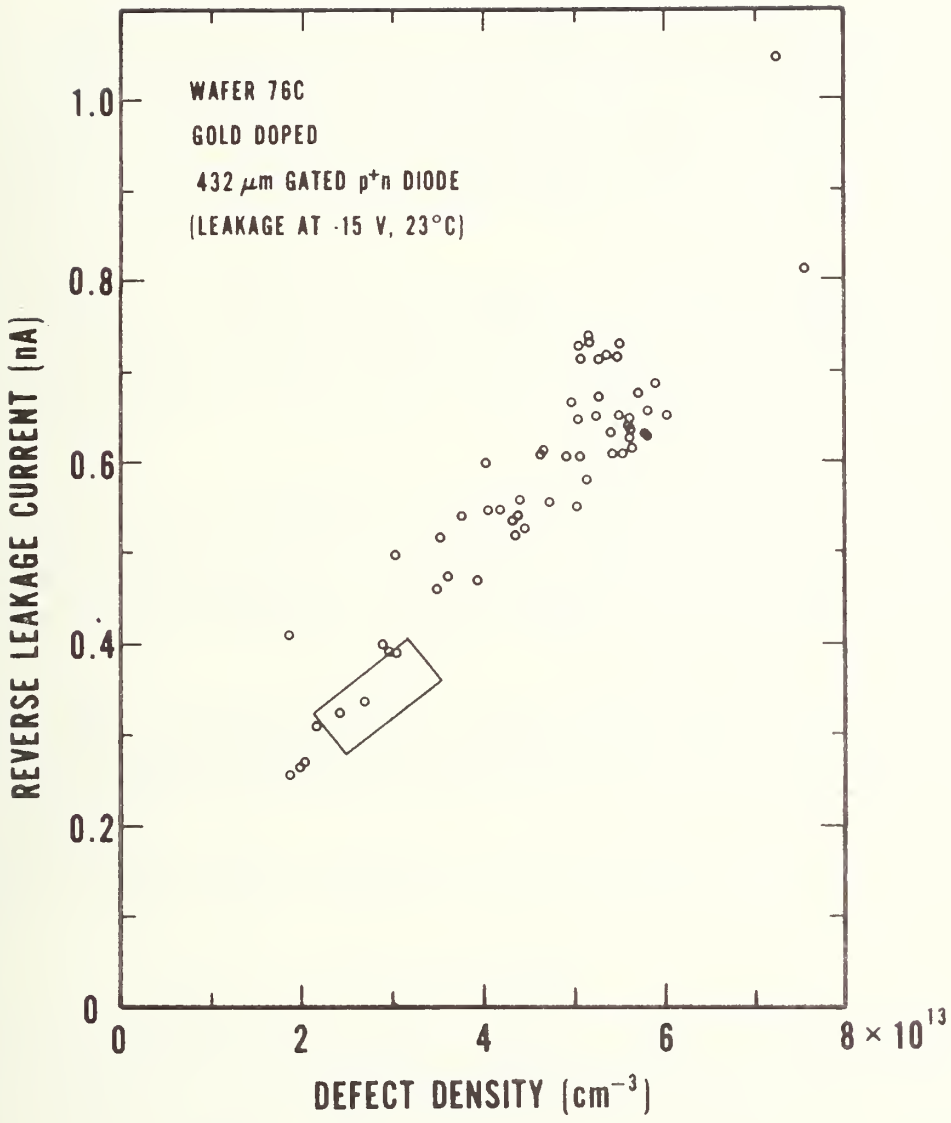

Figure 3-17. Plot of the reverse leakage current versus the acceptor defect density. See text for discussion of the rectangular area.

the same curve as for the p^+n devices (see fig. 3-17), one can infer that the reverse leakage in the n^+p as well as the p^+n is controlled by the midgap acceptor level.

4. SPREADING RESISTANCE MEASUREMENTS

by

J. R. Ehrstein

4.1 Objectives

The overall objective of this task, which began in October 1977, is to increase the reliability with which spreading resistance measurements can be used for radial resistivity screening of thyristor substrate material and for depth resistivity profiling of partially or fully fabricated thyristor structures. The end use for such measurements extends from thyristor fabrication process control to feedback to the design and modeling processes for newer and more advanced thyristor structures. The specific objectives are as follows:

1.1 Develop a silicon surface preparation procedure which enables stable and reproducible spreading resistance measurements to be obtained on bulk (111) *n*-type silicon in the resistivity range (20 Ω·cm to 400 Ω·cm) which covers thyristor substrate material.

1.2 Based on the foregoing, develop a surface preparation procedure for bevel sectioning of thyristor structures which yields improved data quality in the *n*-base layer compared with presently obtainable results while retaining the favorable data character presently obtainable in other regions of the sectioned thyristor.

1.3 Conduct a preliminary test of the equivalence of boron-, gallium-, and aluminum-doped silicon specimens for the calibration of spreading resistance measurements of *p*-type thyristor diffusions.

This report discusses the focus and initial planning stages for this project.

4.2 Background

The ability to measure and to control dopant profiles is important in thyristor structures for a variety of reasons. The state of lateral uniformity of dopant in the high resistivity *n*-type silicon, which later forms the thyristor *n*-base region, determines the reverse blocking voltage which can be achieved. Blocking voltage must be designed around the lowest local resistivity value expected in the *n*-base starting material. Among other thyristor parameters controlled or strongly influenced by dopant profiles are: 1) the contact resistance of the thyristor structure to the metallization which is affected by the electrically active dopant at the surface of the emitter layers, and 2) the on-state injec-

tion efficiency which is affected by the dopant profile in the vicinity of the cathode emitter to p-base junction.

Spreading resistance measurements allow high spatial resolution for both lateral and depth profiling and a large dynamic range of measurable resistivity values as required for depth profiling of graded layers in thyristor, or other semiconductor, structures. It is, however, a comparative technique; resistivity values can be derived from spreading resistance values only after the apparatus has been calibrated against specimens of known resistivity. This calibration is known to depend upon the conductivity type and crystallographic orientation of the specimens, on the surface preparation given the specimens, and possibly upon the dopant species. Further, to derive resistivity values when measurements are made on specimens with vertically graded resistivity, as in diffused layers, a mathematical algorithm is required.

Nevertheless, spreading resistance offers the capability of process control on a routine basis if measurements are reliable and repeatable and if costs and turnaround times are acceptable. It also offers the design or process engineer the possibility of data feedback regarding the profiles obtained by new or modified process cycles. Information of this type should aid in the achievement of very high blocking voltage devices envisioned for high voltage dc transmission systems.

In fact, despite the limitations and difficulties mentioned, spreading resistance measurements have been applied for a number of years to process control, for which there is little published in the literature [4-1], and to feedback for design and modeling purposes [4-2]. Such applications have a longer history for power control devices than for virtually any other type of semiconductor device. Figure 4-1 shows application to screening on incoming high resistivity n-type silicon for uniformity of lateral resistivity for specimens of float-zone-grown and of NTD doped silicon. Figure 4-2 illustrates the manner in which spreading resistance measurements are typically used for thyristor process control. In this figure, short line segments, indicated by numbers 1 to 4, designate allowed limits on position or absolute spreading resistance of key profile features which are known to strongly influence thyristor operation. The position and size of these limits or windows are derived from spreading resistance profiles of properly operating thyristors which are sacrificed to acquire data for these process control limits. In such process-control-related measurements, reference to actual resistivity values obtained through elaborate calibration and/or mathematical algorithms is not required, provided that uncontrolled extraneous variations such as might be due to specimen preparation are eliminated. Of course, for detailed analysis of profiles such as those resulting from new or modified process steps, raw spreading resistance data no longer suffice, and use of calibration data and of mathematical algorithms is required.

In order to assess the current status and limitations of spreading resistance measurements, visits were made to several research and production facilities involved with thyristors. Discussions indicated that insta-

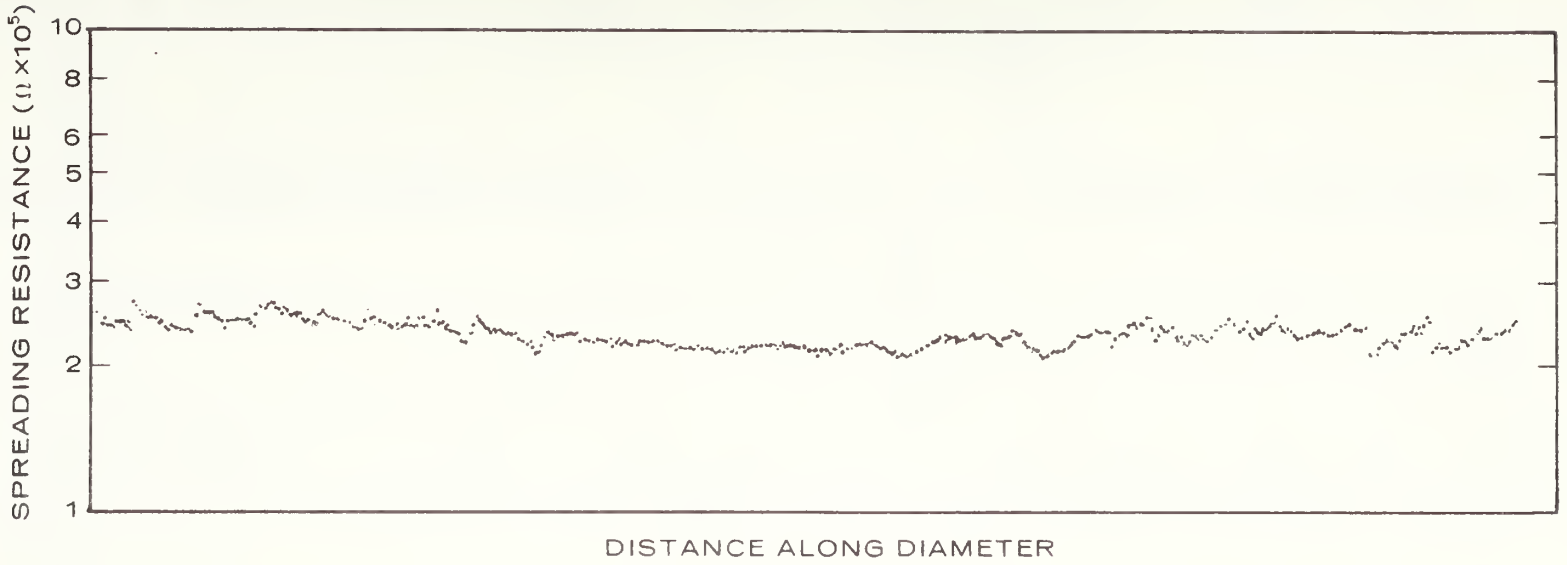

Figure 4-1a. Spreading resistance (resistivity) uniformity across the diameter of an approximately 60-Ω·cm NTD silicon slice.

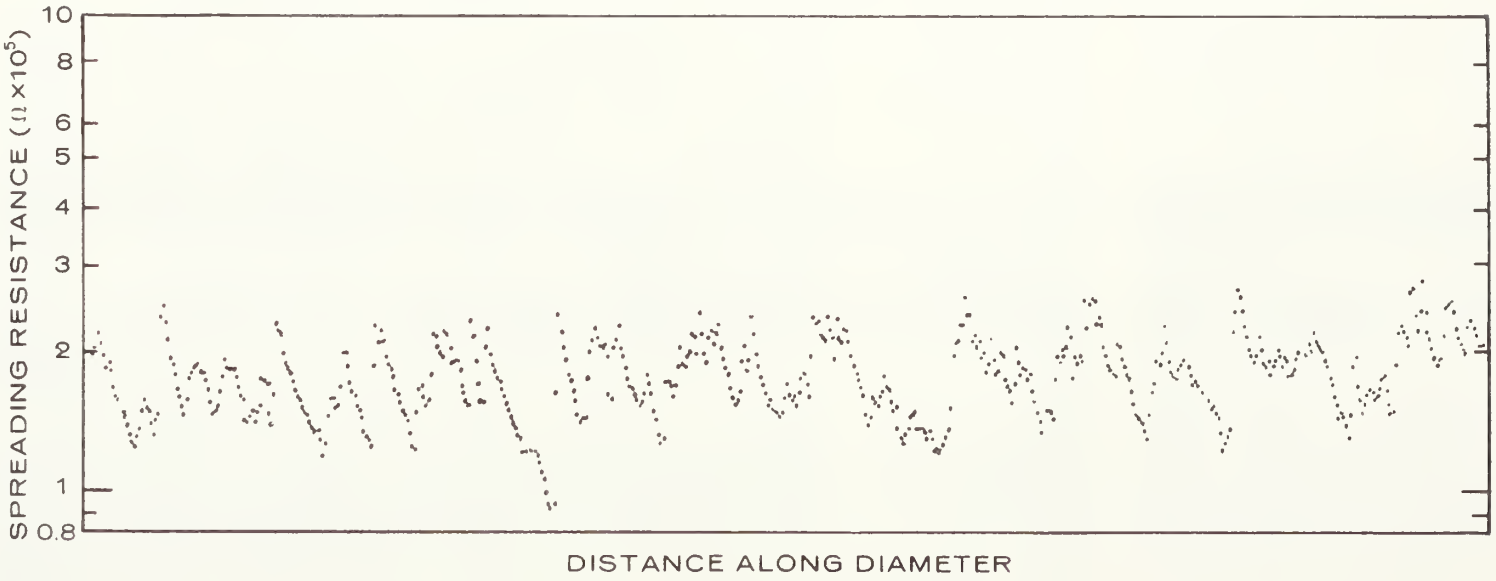

Figure 4-1b. Spreading resistance (resistivity) uniformity across the diameter of an approximately 60-Ω·cm standard float-zoned silicon slice.

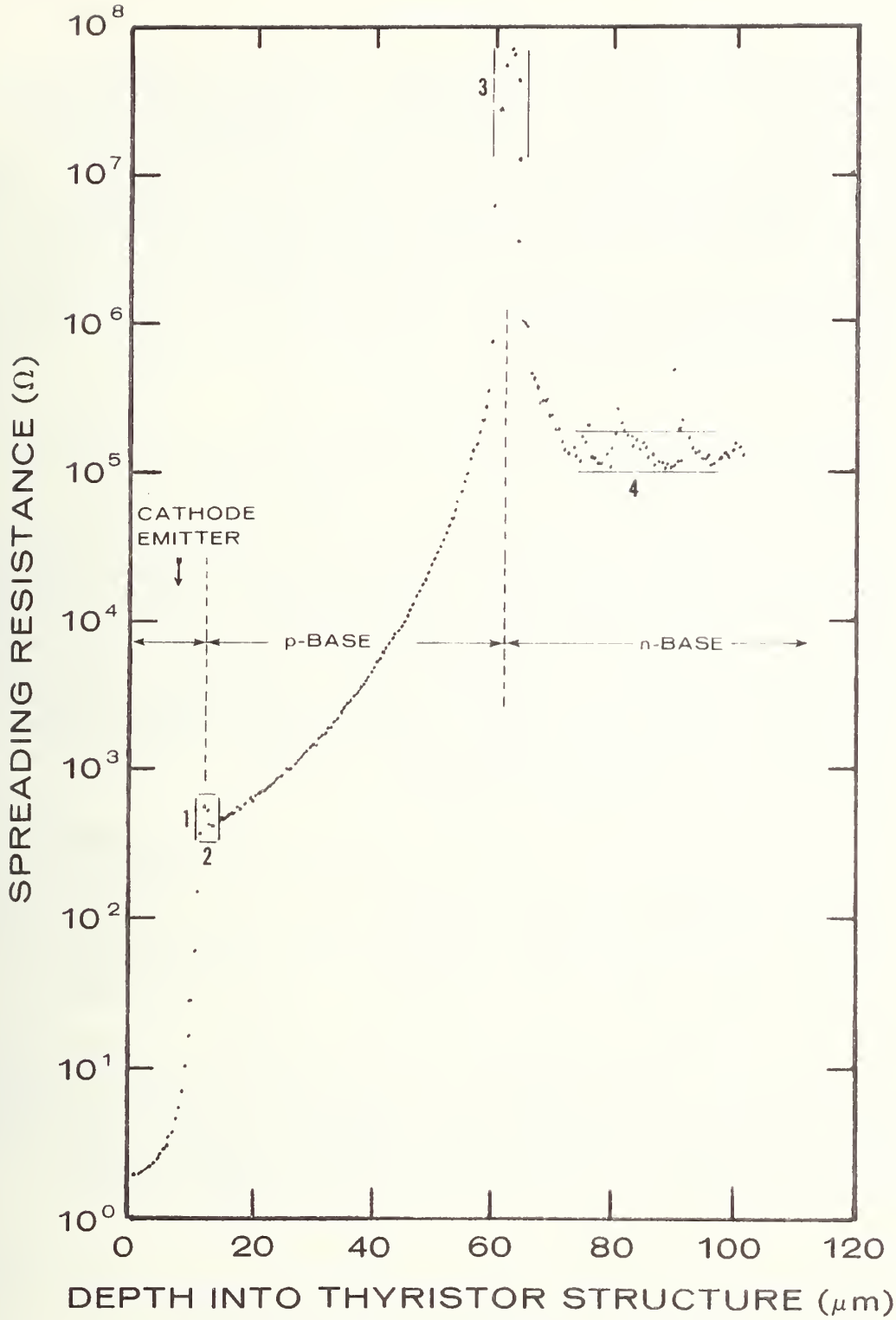

Figure 4-2. Spreading resistance profile of thyristor structure from cathode emitter side. Vertical and horizontal bars show typical process control limits.

bility of spreading resistance measurements on high resistivity *n*-type silicon, whether float-zoned or NTD silicon, is indeed a problem, both during inspection of incoming substrate material and during process control measurements. Discussions also indicated that algorithms for interpretation of spreading resistance depth profile data are available with sufficient speed and accuracy to satisfy current needs. Another area that was identified which merits initial investigation is the validity of the common practice of using boron-doped specimens for calibration of spreading resistance measurements of all *p*-type layers, even those doped with gallium and aluminum.

4.3 Status

4.3.1 Surface Preparation Procedures for Radial Profiling (Objective 1.1)

Several methods, generally based on polishing with diamond compound in nonaqueous fluid, have been selected for surface preparation of high resistivity *n*-type silicon specimens. Aqueous polishes, commonly used for preparation of thyristor specimens, have previously been found to result in erratic and unstable spreading resistance measurements of high resistivity *p*-type silicon [4-3]. Material has been ordered and experiments planned to test reproducibility and stability of spreading resistance as a function of surface preparation. Interfacing of spreading resistance apparatus to a dedicated minicomputer for more efficient data collection and analysis has been completed.

4.3.2 Surface Preparation Procedures for Depth Profiling (Objective 1.2)

No work was performed on this subtask which was planned to follow after initial results are obtained under Objective 1.1.

4.3.3 Dopant Species Dependence of Calibration for *p*-Type Silicon (Objective 1.3)

A search has turned up one supplier of aluminum- and gallium-doped single crystal silicon. The suitability of his material in terms of resistivity uniformity will be tested prior to comparing spreading resistance measurement response on similarly prepared boron-, aluminum-, and gallium-doped specimens at a small number of resistivity values.

5. REFERENCES

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16. ABSTRACT (*A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.*)

This annual report describes NBS activities directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for thyristors and rectifier diodes.

The major tasks under this project are (1) to evaluate the feasibility of the photovoltaic method as a rapid, nondestructive technique for characterizing the resistivity uniformity of high-resistivity, large-diameter silicon wafers, (2) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime controlling or leakage source defects in power grade silicon material and devices, and (3) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

17. KEY WORDS (*six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons*)
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